Scilab Textbook Companion for Op-Amps and Linear Integrated Circuit by S. Sharma[1]

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Book Description

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Scilab numbering policy used in this document and the relation to the above book.

Exa Example (Solved example)

Eqn Equation (Particular equation of the above book)

AP Appendix to Example(Scilab Code that is an Appednix to a particular Example of the above book)

For example, Exa 3.51 means solved example 3.51 of this book. Sec 2.3 means a scilab code whose theory is explained in Section 2.3 of the book.

Contents

List of Scilab Codes

Chapter 1

Differential amplifiers

Scilab code Exa 1.1 Vout and CMMR

```
// chapter 1
//example 1.3
// page no.18,figure no.1.22
//given
Rin1=100;Rin2=100;
Re=2700;Rc=4700;
Hfe=100;
Hie=1000;Hoe=0;
Aid=(Hfe*Rc)/(Rin1+Hie);
disp(Aid)//differential gain
//Acm=(2*Re*Hoe-Hfe)*Rc/(2*Re(1+Hfe)+(Rin1+Hie)(1+2*
    Re*Hoe)),and Hoe=0
x=2*Re*1+2*Re*Hfe+Rin1+Hie;
Acm=-(Hfe*Rc)/x;
disp(Acm)//neglecting the negative value.taking mod
    of Acm
Acm=-(Acm)
CMRR=20*log10(Aid/Acm);
disp(CMRR)//is in db
Rin=2*Rin1+2*Hie;
disp(Rin)//input resistance
```

```
Ro=Rc
disp(Ro)//output resistance
```

Scilab code Exa 1.2 Icq and Vceq

```
// chapter 1
// example 1.2
//page 17. figure 1.21
//given
Rc=4700,Re=2700;// Resistor is in ohm
Vcc=12;Vee=12;// voltage is in volt
Vbe=.7;// assuming Vbe
Ie=(Vee-Vbe)/(2*Re);
disp(Ie)//current is in ampere
Icq=Ie;
disp(Icq)//current is in ampere
Vc=Icq*Rc;
Vce=Vcc+Vbe-Vc;
disp(Vce)
```

Scilab code Exa 1.3 Aid and Acm and CMRR and Ri and Ro

```
// chapter 1
// example 1.3
//page 18
Rin1=100;Rin2=100;Re=2.7*10^3;Rc=4.7*10^3;
hfe=100;hie=1000;hoe=0;
Aid=(hfe*Rc)/(Rin1+hie);//Differential gain
disp(Aid)
Acm=((2*Re*hoe-hfe)*Rc)/(2*Re*(1+hfe)+(Rin1+hie)
    *(1+2*Re*hoe));//comman mode gain
Acm=-Acm// neglecting negative sign
disp(Acm)
```

```
CMRR=Aid/Acm
CMRR=20*log10(CMRR);
disp(CMRR)
Rin=2*(Rin1+hie)//input resistance
Ro=Rc//output resistance
```

Scilab code Exa 1.4 constant current I

```
//chapter 1
//example 1.4
// page 23,figure 1.27
Vee=10;R1=2400;R2=2400;R3=1000;Vbe=.7;//given
I=(Vee-(R2*Vee/(R1+R2))-Vbe)/R3;
disp(I)// result is in ampere
```

Scilab code Exa 1.5 value of RE

```
//chapter 1
// example 1.5
//page 27.figure 1.31
Ic1=10*10^-6;Vcc=50;Vbe=.7;R=50*10^3;
Ic2=(Vcc-Vbe)/R;
disp(Ic2);
Vt=26*10^-3// assume at room temperature of 300k
Re=Vt/Ic1*log(Ic2/Ic1);
disp(Re)//result in ohm
```

Scilab code Exa 1.6 common mode op voltage and differential mode output

```
//chapter 3
// exmaple 3.6
//page 124 , figure 3.17
R1=1*10^3;R2=R1;R3=R1;//given
Rf=1*10^3;//given
Vin1=2;Vin2=1;Vin3=4;//given
Vout=-((Rf/R1)*Vin1+(Rf/R2)*Vin2+(Rf/R3)*Vin3);
disp(Vout)
```

Scilab code Exa 1.7 Dc bias point and ip and op resistance

```
//chapter 1
// example 1.7
//page 32,figure 1.36
Vee=12;Vbe=0.7;Rin=100;Re=8400;Rc=3900;Vcc=12;
Xdc=100// dc gain
Icq=(Vee-Vbe)/((Rin/Xdc)+2*Re);
Vceq=Vcc+Vbe-Icq*Rc;
disp(Vceq,Icq)//the DC base point or Q point is at(
   volt,ampere)
Hie=1100// assuming
Ri=2*(Rin+Hie);//input resistance
disp(Ri)// input resistance in ohm
Ro=Rc// output resistance
```

Scilab code Exa 1.8 Icq and Vceq voltage gain ip and op resistance

```
//chapter 1
// example 1.8
// page 33, figure 1.37:
Xdc=100;Xac=100;//AC and DC gain
Vbe=0.7;Vee=10;Vcc=10;// voltage is in volts
Re=4700;Rin=50;Rc=2700;//resistance in ohm
```

```
Hfe=100;Hie=1100// assuming
Icq=(Vee-Vbe)/(2*Re+(Rin/Xdc));
disp(Icq)//result current
Vceq=Vcc+Vbe-Rc*Icq;
disp(Vceq)// result voltage
Aid=(Hfe*Rc)/(2*(Rin+Hie));//voltage gain Aid
disp(Aid)
Ri=2*(Rin+Hie)// input resistance
disp(Ri)//in ohm
Ro=Rc;// output resistance
disp(Ro)//ohm
```

Scilab code Exa 1.9 operating point voltage gain ip and op resistance

```
// chapter 1
// example 1.9
//page 34, figure 1.38
Xdc=100;Xac=100;// gain
Vbe=0.7;Vee=12;Vcc=12;//given voltage in volts
Re=4700;Rin=50;Rc=2700;// given resistance in ohm
Hfe=100;Hie=1100;// given
Icq=(Vee-Vbe)/(2*Re+(Rin/Xdc));
Vceq=Vcc+Vbe-Rc*Icq;
disp(Icq,Vceq)//operating point(volt,ampere)
Aid=(Hfe*Rc)/(Rin+Hie);// voltage gain
disp(Aid)// result
Ri=2*(Rin+Hie)// input resistance
disp(Ri)//in ohm
Ro=Rc;// output resistance
disp(Ro)//output resistance in ohm
```

Scilab code Exa 1.10 operating point voltage gain ip and op resistance

```
// chapter 1
// example 1.10
//page 34, figure 1.39
Xdc=100;Xac=100;// gain
Vbe=0.7;Vee=12;Vcc=12;//given voltage in volts
Re=8200;Rin=150;Rc=3300;// given resistance in ohm
Hfe=100;Hie=1000;// given
Icq=(Vee-Vbe)/(2*Re+(Rin/Xdc))
Vceq=Vcc+Vbe-Rc*Icq
disp(Icq,Vceq)//operating point(volt,ampere)
Aid=(Hfe*Rc)/(Rin+Hie);// voltage gain
disp(Aid)// result
Ri=2*(Rin+Hie)// input resistance
disp(Ri)//in ohm
Ro=Rc;// output resistance
disp(Ro)//output resistance in ohm
```

Scilab code Exa 1.11 output voltage and CMRR

```
//chapter 1
// example 1.11
// page 35
Rin=1000;Rc=1000;Re=2500000;// resistance is in ohm(
    given)
Hfe=50;Hre=0;Hoe=0;Hie=1000;//given
Vid=1*10^-3;Vc=20*10^-3// voltage in volts
Aid=-(Hfe*Rc)/(Rin+Hie);// differential gain Aid
Vout=Aid*Vid;// output voltage
disp(Vout)//result in ampere.
// to calculate CMRR we have to first find Acm
    common mode gain
Acm=((2*Re*Hoe-Hfe)*Rc)/(2*Re*(1+Hfe)+Rin+Hie)//
    common mode gain
CMRR=Aid/Acm;//CMRR
disp(CMRR)//result
```

```
CMRRdb=20*log10(CMRR);
disp(CMRRdb)// result CMRR is in db
```

Scilab code Exa 1.12 DC characteristics

```
// chapter 1
// example 1.12
// page no.38, figure 1.44
Kn1=.2*10^-3;Kn2=.2*10^-3;Kn3=.4*10^-3;Kn4=.4*10^-3; // all in mA/V^2
Vtn=1;Vcc=12;Vee=-12;// voltage is in volts
R1=27000;Rd=15000;
// calculation of I1 and Vgs4
// applying KVL=> Vcc-Vee=I1*R1+Vgs4-------------eq(1)
// I1=Kn3*(Vgs4-Vtn)^2-----------eq(2)
// put eq (2) in eq (1)
//((Vcc-Vee)-Vgs4)/R1=Kn3*(Vgs4-Vtn)^2
p1=poly([-13.2 -20.6 10],'Vgs4','c');
roots(p1)// we have to take only value positive and greater than Vtn
I1=Kn3*(2.573-Vtn)^2;//only positive and value greater than Vtn of  Vgs4 taken
disp(I1)
//calculation  of drain current Iq
Iq=I1;// identical M4 and M3
disp(Iq)
// calculation of Id1 and Id2
Id1=Iq/2;
Id2=Iq/2;
disp(Id1,Id2)// identical
// calculation of gate voltage for M1 and M2
Vgs1=Vtn+sqrt(Id1/Kn1);// using Id1=Kn1*(Vgs1-Vtn)^2
disp(Vgs1)// result gate to source voltage
Vgs2=Vgs1;// since they are identical
```

```
disp(Vgs2)
//calculation of Vout1 and Vout2
Vout1=Vcc-Id1*Rd;
disp(Vout1)// under quiescent condition
Vout2=Vcc-Id2*Rd;
disp(Vout2)
// calculation of maximum common mode input voltage
    Vcmmax
Vds1=Vgs1-Vtn;
Vcmmax=Vout1-Vds1+Vgs1;//maximum common mode voltage
disp(Vcmmax)// result is in volts
// calculation of minimum common mode input voltage
    Vcmmin
Vds4=Vgs2-Vtn;
Vcmmin=Vgs1+Vds4-Vcc;// minimum common mode input
    voltage
disp(Vcmmin)// volts
```

Scilab code Exa 1.13 Aid Acm CMRR

```
// chapter 1
// example 1.13
// page 44, figure 1.52
Rl=%inf;B=100;Rin=0;
Re=1;// let suppose
Iq=4*10^-3;
Vt=26*10^-3;Va2=150;Va4=100;
I2=Iq/2;
I4=Iq/2;
disp(I2,I4)
Gm=Iq/(2*Vt);//parameters
Ro2=Va2/I2;
Ro4=Va4/I4;
Aid=Gm*((Ro2*Ro4)/(Ro2+Ro4));//Aid =Gm(Ro2||Ro4||Rl)
    ,Rl=%inf
```

```
disp(Aid)// differential mode gain Aid
r=(2*(B*Vt))/Iq// Vt=26mV at 300k
//Re=1/X*Iq and Rc=1/x*Iq/2
//Rc/Re=2
Rc=2*Re;
//assuming 2*(1+B)*Re/(r+Rin)>>>>1
//Acm=((-Gm*Rc)/1+((2*(1+B)*Re)/(r+Rin)));
k=(2*(1+B)*Re)/((r+Rin)/1000)
Acm=-((Gm*Rc)*1000)/k;
disp(Acm)// common mode gain
CMRR=Aid/-Acm;
disp(CMRR)//
CMRRdb=20*log10(CMRR);
disp(CMRRdb)// result is in db
```

Scilab code Exa 1.14 voltage gain and ip resistance and operating point

```
// chapter 1
//example 1.14
// page 46, figure1.54
Bac=100;Bdc=100;
Vbe=.715;Vd1=.715; Vz=6.2;Vee=-10;Vcc=10;Vt
   =26*10^-3;// at room temprature
Re=2700;Rin=10000;Rc=4700;//assuming Rin= 10k
Izt=41*10^-3;
Vin=0;// for dc analysis
//calculation of the value of Ie,Icq1 and Icq2
Vb3=Vee+Vz+Vd1
Ve3=Vb3-Vbe
Ie=(Ve3-Vee)/Re;
disp(Ie)
Ie1=Ie/2
Ie2=Ie/2
A=B/(1+B);
Icq=A*Ie1;//(B/(B+1))*Ie1
```

```
disp(Icq)
Icq2=Icq;
disp(Icq2)
Gm=Icq/Vt// Vt at room temp 26mA
r=(B*Vt)/Icq
Ib=Icq/B
Ve1=-Ib*Rin-Vbe;
disp(Ve1)//result
Vc1=Vcc-Icq*Rc;
disp(Vc1)
Vceq=Vc1-Ve1;
disp(Vceq,Icq)//result operating point
```

Scilab code Exa 1.15 collector current

```
//chapter 1
// example 1.15
//page 47, figure 1.57
Bdc=100;Bac=100;
Vbe=.715;
R=5600;
Vr=-(Vbe-10);
Ir=Vr/R;// Ir=Ic+Ib=Vr/R
disp(Ir)
Ic=Ir*(Bdc/(1+Bdc));//Ir=Ic+Ib=Ic+Ic/Bdc
disp(Ic)//ampre
Ic2=Ir
Ic3=Ir
Ic4=Ir
```

Scilab code Exa 1.16 smallest and largest possible value of current

```
//chapter 1
```

```
//example 1.16
//page 48,figure 1.59
Ie=400*10^-6;
Bmin=80;Bmax=120;
//Ie=Ie1+Ie2   for identical transistor Ie1=Ie2
Ie1=Ie/2
Ie2=Ie/2
IB1max=Ie1/(1+Bmin)
IB2max=Ie2/(1+Bmin)
IBmax=(IB1max+IB2max)/2;
disp(IBmax)//largest input bais current
IB1min=Ie1/(1+Bmax)
IB2min=Ie2/(1+Bmax)
IBmin=(IB1min+IB2min)/2;
disp(IBmin)// smallest current
Iios=IBmax-IBmin// input bais current
disp(Iios)//result
```

Scilab code Exa 1.17 Ri Ro differential and common mode voltage gain

```
//chapter1
//example 1.17
//page 49, figure 1.60
I=.2*10^-3; B=200;Va=100;Rl=%inf;
Vt=26*10^-3//assuming at room temprature
I2=I/2
I4=I2
r02=Va/I2;
disp(r02)
r04=Va/I4;
disp(r04)
Gm=2/Vt
Aid=Gm/((1/r02)+(1/r04)+(1/Rl));
disp(Aid)
Ri=2*(B/I)//Ri=2*r
```

```
disp(Ri)
Ri=(r02*r04)/(r02+r04);
disp(Ri)
```

Chapter 2

Operational amplifier characteristic

Scilab code Exa 2.1 value of R1

```
//chpter 2
// example 2.1
//page 63, figure 2.16
//design the value of R1 if output voltage level
   required is zero volts.
// given
Vout=0
Vin=6.84
Vbe=0.7
R2=270
//Vin-Vbe-I(R1+R2)=0 applying KVL to base emitter
I=(Vin-Vbe)/(R1+R2)
Vout=I*R2;
R1=1657.8-270;  // 0=(6.84-.7)270/(270+R1)
disp(R1) // results
```

Scilab code Exa 2.2 input bais current and input offset current

```
//chapter 2
//example 2.2
//page 70
Ib1=18*10^-6 ;Ib2=22*10^-6;// given
Ib=(Ib1+Ib2)/2 //input base current
disp(Ib) //result
Iios=(Ib2-Ib1) // input offset current
disp(Iios)// result
```

Scilab code Exa 2.3 Compensating network

```
//chapter 2
//example 2.3 page 76
//figure 2.36
Vios=8*10^-3;V=12;Vcc=12;Vee=12;//given
Rc=10;//let choose Rc less than 100 ohm
Rb=(V*Rc)/Vios //Vios=(Rc/Rb)*V
Rmax=Rb/10// let choose
Ra=Rmax*4;
disp(Ra)//thus resistance Ra is potentiometer which
   can be adjusted till output reaches zero value
```

Scilab code Exa 2.4 Total output offset and compensating resistance

```
//chapter 2
//example 2.4 page 79
//figure 2.40
Vios=12*10^-3; Rf=100*10^3;R1=10*10^3; Ib=500*10^-9;
   Iios=90*10^-9;//given
R3=Rf/R1;R4=R3+1;
Voos=Vios*R4+Rf*Ib;
```

```
disp(Voos)
Rcomp=R1*Rf/(R1+Rf);//Rcomp=R1||Rf
disp(Rcomp)
Voos2=Vios*R4+Rf*Iios;//with Rcomp,the output offset voltage become
disp(Voos2)
```

Scilab code Exa 2.5 change in output voltage

```
//chapter 2
//example 2.5 page 83
T=55-25;//chnage in temperature
A=150;//gain
Vios=.15*10^-3;//input offset voltage shift=chnage in output voltage/change in temp
Voos=Vios*T;//Vios=Voos/T
disp(Voos)
Vout=A*Voos;
disp(Vout)
```

Scilab code Exa 2.6 error voltage and output voltage

```
//chapter 2
//example 2.6 page83
Rf=100*10^3;R1=1*10^3//given
Viovd=14*10^-6;//input offset voltage drift
Iiocd=.5*10^-9;//input offset current drift
Vin=7*10^-3;
T=45-25;//change in tempreture
R2=Rf/R1;R3=R2+1;
Ev=R3*Viovd*T+Rf*Iiocd*T;//error voltage
disp(Ev)
A=-Rf/R1;//gain
```

```
Vout=A*Vin+Ev
Vout=A*Vin-Ev
```

Chapter 3

Basic application of Op amps

Scilab code Exa 3.1 voltage

```
//chpater 3
// example 3.1
//page 106, figure 3.3
R1=10000;Rf=47000;//given
Af=-(Rf/R1);// voltage gain Af=Vout/Vin
disp(Af)//negative sign indicate phase shift between
    input and output
```

Scilab code Exa 3.2 value of Rf

```
//chapter 3
//example 3.2
//page 107
R1=4700;
Af=-60;
Rf=Af*R1//voltage gain Af=-Rf/R1
disp(Rf)//result
```

Scilab code Exa 3.3 voltage gain ip and op resistance bandwidth

```
//chapter 3
// example 3.3
//page 112
A=2*10^5;//open loop gain
Rin=2*10^6;// input resistnace
Ro=75;// output resistance
Fo=5;// single break frequency in herzt
R1=470;Rf=4700;
K=Rf/(Rf+R1)
B=R1/(R1+Rf)
Af=-(A*Rf)/(R1+Rf+R1*A);//close loop gain
Rinf=R1+(Rf*Rin)/(Rf+Rin+A*Rin);
disp(Rinf)//close loop resistance
Rof=Ro/(1+A*B);//close loop output resistance
disp(Rof)//output resistance
Ff=Fo*(1+A*B);
disp(Ff)//bandwidth with feedback
```

Scilab code Exa 3.4 feedback resistance Rf

```
//chapter 3
// example 3.4
//page 114,figure 3.9
R1=1000;
Af=61;//closed loop gain
Rf=R1*(61-1);//Af=1+(Rf/R1)
disp(Rf)//feedback resistance
```

Scilab code Exa 3.5 close loop gain ip and op resistance and bandwidth

```
//chapter 3
//example 3.5
//page 120,
A=2*10^5;//open loop gain
R1=1000;Rf=10000;
Ri=2*10^6;//input resistance
Ro=75;//output resistance
Fo=5;// single break frequency in Hz
B=R1/(R1+Rf)
Af=A/(1+A*B);//gain
disp(Af)// closed loop gain
Rif=Ri*(1+A*B);// closed loop input resistance
disp(Rif)
Rof=Ro/(1+A*B);
disp(Rof)// colsed loop output resistance
Fof=Fo*(1+A*B);
disp(Fof)// colsed loop bandwidth in Hz
```

Scilab code Exa 3.6 output voltage

```
//chapter 3
// exmaple 3.6
//page 124 , figure 3.17
R1=1*10^3;R2=R1;R3=R1;//given
Rf=1*10^3;//given
Vin1=2;Vin2=1;Vin3=4;//given
Vout=-((Rf/R1)*Vin1+(Rf/R2)*Vin2+(Rf/R3)*Vin3);
disp(Vout)
```

Scilab code Exa 3.7 practical integrator

```
// chapter 3
// example 3.7
//page 135
A=10;//d.c gain
R1=10000;
F=10000;//input frequency
CfRf=15915*10^-4;
Fa=F/A;
Rf=10*R1;// A=Rf/R1
//Fa=1/(2*3.14*Rf*Cf)
Cf=15915*10^-4/Rf;
disp(Cf)
Rcomp=(R1*Rf)/(R1+Rf);
disp(Rcomp)
```

Scilab code Exa 3.8 maximum change in output voltage and slew rate

```
//chapter 3
//example 3.8
//page 136, figure 3.35
F=1000;
R1=1000;Cf=.1*10^-6;
Vin=5;//voltage in V
T=1/F;//time period
disp(T)// in second
Vout=(Vin*T)/(2*R1*Cf);// change in output voltage
disp(Vout)//given saturation level is 14V hence
    output will not saturate will be triangular in
    nature
S=2*%pi*F*Vin;// slew rate
disp(S)//minimum slew rate
```

Scilab code Exa 3.9 safe frequency DC gain

```
//chapter 3
//example 3.9
//page 137
R1=120*10^3;Rf=1.2*10^6;Cf=10*10^-9// given
fa=1/(2*%pi*Rf*Cf);// corner frequency
F=10*10^3;
Vin=5;
disp(fa)//coner frequency
safefrequency=10*fa//safe frequency is 10 times of
    corner frequency
Adc=Rf/R1;//D.C gain
Adb=20*log10(Adc)// gain in db
A=(Rf/R1)/sqrt(1+(F/fa)^2)//gain for practical
    intregrater circuit
disp(A)
Vout=A*Vin;//|A|=Vout(peak)/Vin(peak)
disp(Vout)
```

Scilab code Exa 3.11 design practical differentiator

```
//chapter 3
//example 3.11
//page 147
fa=150;fmax=150;//given
C1=1*10^-6;// assuming
Rf=1/(fa*2*%pi*C1);//fa=1/2piRfC1
disp(Rf)
fb=10*fa;// safe frequency
disp(fb)
R1=1/(2*%pi*fb*C1);//fb=1/2piC1R1
disp(R1)
Cf=((R1*C1)/Rf);//using R1C1=RfCf
disp(Cf)
Rcomp=(R1*Rf)/(R1+Rf);//rcomp=R1||Rf
disp(Rcomp)// generally Rcomp is selected equal to
```

R1

Scilab code Exa 3.15 scaling adder circuit

```
//chapter 3
// example 3.15
//page 148
// Vout=-(3Vin1+4Vin2+5Vin3)
Rf=120*10^3;
// for inverting summer we have Vout=-(Rf/R1Vin1+Rf/
    R2Vin2+Rf/R3Vin3)
R=Rf/3;//Rf/R1=3  comparing the cofficients
disp(R1)
R2=Rf/4;
disp(R2)
R3=Rf/R3;
disp(R3)
```

Scilab code Exa 3.16 op amp circuit

```
//chapter 3
// example 3.16
// page 149
// Vout=2Vin1-3Vin2+4Vin3-5vin4
Rf1=100*10^3
// Vout1=-(Rf1/R1Vin1+Rf1/R3Vin3)
R1=Rf1/2;// Rf1/R1=2  comapring the cofficient
R3=Rf1/4:
disp(R1,R2)
Rf2=120*10^3
// Vout2=-(Rf2/R2Vin1+Rf2/R4Vin3)
R2=Rf2/3;
R4=Rf2/5;
```

```
disp(R2,R4)
// output of subtracter is Vout=Vout2-Vout1
```

Scilab code Exa 3.17 find ratio of Vout by Vin

```
// chapter 3
// example 3.17
//page 150, figure 3.53
Ri=%inf;Ro=0;
Aol=%inf;
Vb=0;//b is virtually ground
Vout=1;// let us assume
//input current of op-amp is zeroas R=%inf
I1=(Vb-Vout)/100000
If2=I1;
Va=((10000)/(100000))*(Vb-Vout)
//at node A Iin=I1+If1
// (Vin-Va)/10*10^3=(Va-Vb)/10*10^3 + (Va-Vo)
    /100*10^3
Vin=Va+(10000)*((Va/10000)+((Va-Vout)/100000));
Ratio=Vout/Vin// result ratio of Vout/Vin
```

Scilab code Exa 3.18 output voltage in term of Vin1 and Vin2

```
// chapter 3
//example 3.18
// page 150, figure 3.55
Rf=10*10^3;R1=100*10^3;
Rf1=100*10^3;R11=10*10^3;
Vin1=1;// let suppose
Vin2=2
Vout1=(1+(Rf/R1))*Vin1;// 1st stage is non inverting
    amplifier
```

```
disp(Vout1)
// second stage there are two input Vout1 and Vin2
   aplly superposition theorem
Vout2=-(Rf1/R11)*Vout1;
//with Vout1 grounded,Vin2 active ,it behave as non-
   inverting amplifier
Vout3=(1+(Rf1/R11))*Vin2;
Vout=Vout2+Vout3;
disp(Vout)
```

Scilab code Exa 3.19 range of gain

```
// chapter 3
//example 3.19
//page 163, figure 3.73
R1=200;R2=100;Rf=100*10^3;//given
Rg1=100+0;//potentiometer resistance is 0 at start
gain1=((1+2*(Rf/Rg1))*(R2/R1));
Rg2=100+100*10^3;//potentiometer maximum value
gain2=((1+2*(Rf/Rg2))*(R2/R1));
disp(gain1,gain2)// range of gain
```

Scilab code Exa 3.20 Value of Rg

```
// chapter 3
// example 3.20
//page 164,figure 3.74
R1=100*10^3;R2=100*10^3;Rf=470;//given
// gain=(1+2Rf/Rg)(R2/R1)
gain=100;//given
Rg=(((gain/(R2/R1))-1)\(2*Rf));
disp(Rg)//result for Rg so that gain is 100
```

Scilab code Exa 3.21 transduer resistance

```
//chapter 3
//example 3.21
//page 167
Ro=100;
x=0.00392;
T1=25;//temp at 25c
R(25)=Ro*(1+(x*T1));
disp(R(25))// resistance at 25 degree
T2=100;
R(100)=Ro*(1+(x*T2));
disp(R(100))//resistance at 100 degree
```

Chapter 4

Non linear application of op amps

Scilab code Exa 4.1 threshold voltage

```
// chapter 4
//example 4.1
// page 193 ,figure 4.20
R1=120;R2=51*10^3;//given
Vsat=15;Vcc=15;Vee=15;Vin=1;//given
Vut=((Vsat*R1)/(R1+R2));
disp(Vut)//result threshold in ampere
Vult=((-Vsat*R1)/(R1+R2));
disp(Vult)//ampere
```

Scilab code Exa 4.2 Calculate value of R1 and R2

```
//chapter 4
//example 4.2
//page 193,figure 4.21
Vsat=12;Vh=6;
```

```
// Vh=(R1/R1+R2)(Vsat-(-Vsat))
R1=10000;// let assume
x=(Vh/(Vsat-(-Vsat)));
disp(x)
R2=((1-.25)*R1)/.25
disp(R2,R1)
```

Scilab code Exa 4.3 time duration

```
// chapter 4
// example 4.3
// page 194
Vp_p=5;//peak to peak volatage of sine wave
Vlt=-1.5;//lower threshold level
Vh=2;// hysteresis width
f=1000;
Vut=Vh-(-Vlt);
disp(Vut)
Vm=Vp_p/2;
disp(Vm)
//Vlt=Vm*sin(%pi+x)
x=36.87;// taking sin invers
T=1/f;
disp(T)
T1=(T*(180+x))/360;//T1 exist for angle 0 to (180+36.87)
disp(T1)
T2=T-T1;//t2 exist for angle 216.87 to 360
disp(T2)
```

Scilab code Exa 4.4 calculate Vlt Vut and Vh

```
// chapter 4
```

```
//example 4.4
//page 196
Vsat=12;
R1=1000;R2=3000;//given
Vlt=(-(+Vsat)*R1)/R2;
disp(Vlt)// lower threshold
Vut=(-(-Vsat)*R1)/R2;//upper threshold
disp(Vut)
Vh=(R1/R2)*(Vsat-(-Vsat));//hysteresis width
disp(Vh)
```

Scilab code Exa 4.5 change in output voltage

```
// chapter 4
// example 4.5
//page 220
Vin=5;
FRR=80;
Vout=Vin/10^4*log10(10);// FRR=20log(Vin/Vout)
disp(Vout);//change in output voltage
```

Chapter 6

Operational Transconductance Amplefier

Scilab code Exa 6.1 calculate frequency

```
//chapter 6
// example 6.1
//page 246
Gm=55*10^-6;
C=8.75*10^-12;
Fh=Gm/(2*3.14*C);//Fh=f-3db
disp(Fh)//result
```

Chapter 7

waveform generator

Scilab code Exa 7.1 calculate Vlt Vut and frequency of oscillation

```
//chapter 7
//example 7.1
//page 259
R1=86*10^3;R2=100*10^3;
Vsat=15;Rf=100*10^3;
C=.1*10^-6;
Vut=(R1*Vsat)/(R1+R2);
disp(Vut)// upper threshold
Vlt=(R1*(-Vsat))/(R1+R2);
disp(Vlt)//lower threshold
fo=1/(2*Rf*C)*log((Vsat-Vlt)/(Vsat-Vut));
disp(fo)
```

Scilab code Exa 7.2 T equal to 2RfC

```
//chapter7
// example 7.2
//page 259
```

```
R2=%s
R1=.86*R2
Vsat=%s
Rf=%s;
C=%s;
y=(Vsat-(R1*(-Vsat))/(R1+R2))/(Vsat-(R1*Vsat)/(R1+R2
   ))
g=2.72;//g=y=5.0592/1.86
T=2*Rf*C*log(g)// Rf=C=%s
disp(T)// %s*%s=s same as 2*Rf*C=2s
```

Scilab code Exa 7.3 frequency of oscillation

```
// chapter 7
// example 7.3
// page 276
R3=6000;R4=2000;//given
R=5100;
C=.001*10^-6;
A=1+(R3/R4);
if A>3 then
  f=1/(2*3.14*R*C)
   disp(f)//frequency of oscillation
 end
```

Scilab code Exa 7.4 wien bridge oscillator

```
//chapter 7
//example 7.4
//page 277
C=.05*10^-6;// let choose capacitor C<1uf
C1=C;C2=C;
f=1000;
```

```
R=1/(2*3.14*f*C);
disp(R)
//for proper operation gain of non inverting op—amp
   must be 3
R4=%s
R3=R4*(3-1);//1+R3/R4=3
disp(R3)
R4=10000;// assume
R3=2*R4
disp(R3,R4)
```

Scilab code Exa 7.5 triangular waveform

```
//chapter 7
//example 7.5
// page 280
Vsat=15;
Vout=7.5;
fo=5000;
R2=10*10^3;//let assume (use a 50k POT)
R3=(2*Vsat*R2)/Vout;
disp(R3)
C=.01*10^-6;//let assume
R1=R3/(4*C*R2*fo);//fo=R3/4R1C1R2
disp(R1)
```

Scilab code Exa 7.6 output frequency

```
//chapter 7
//example 7.6
//page 285, figure 7.40
R1=10000;R2=5100;R3=10000;
C1=.001*10^-6;
```

```
V=10;
V5=(V*R3)/(R3+R2);
disp(V5)
fo=2.4*(V-V5)/(R1*C1*V);
disp(fo)
```

Scilab code Exa 7.7 monoshot using 741

```
//chapter 7
//example 7.7
// page 286,figure 7.42
R1=10000;R2=10000;
Vd1=.7;//diode drop
Vsat=12;//supply voltage
TP=2*10^-6;
C=.5*10^-9;
B=R1/(R1+R2)
//T=RCln((1+Vd1/Vsat)/(1-B))
k=((1+(Vd1/Vsat))/(1-B))
h=log(k)
R=TP/(C*h)
```

Chapter 8

Timer IC and Application

Scilab code Exa 8.1 output pulse width

```
// chapter 8
//example 8.1
//page 293
R=10*10^3;C=.1*10^-6;// given
t=1.1*R*C;//output pulse width
disp(t)//pulse widht in sec
```

Scilab code Exa 8.2 output frequency and duty cycle

```
//chapter 8
//example 8.2
//page 298
R1=4*10^3;R2=4*10^3;// given for 555 timer
C=.01*10^-6;//for 555 timer
f=1.44/((R1+2*R2)*C);
disp(f)//frequency of output in Hz
D=(R1+R2)/(R1+2*R2);
disp(D)//duty cycle
percentage=D*100
```

Scilab code Exa 8.3 timer

```
//chapter8
//example 8.3
//page300
Ton=5;//given
C=10*10^-6;//let assume
R=Ton/(1.1*C);//using Ton=1.1RC
disp(R)//this not standard value but we can adjust
    by connecting variable resistance
```

Scilab code Exa 8.4 design an astable multivibrator

```
//chapter 8
//example 8.4
//page 301
Toff=1;Ton=3;//given
C=10*10^-6;//choosing
R2=Toff/(.693*C);//using eq Toff=.693RC
disp(R2)//resistance
//Ton=.693(R1+R2)C
R1=(Ton/(.693*C))-R2;
disp(R1)//required resistance
```

Scilab code Exa 8.5 circuit design

```
//chapter8
//example8.5
//page301
```

```
T=10*10^-3;//for proper operation of LED which remain ON for 10msec
C=.22*10^-6//choose
Vcc=15;Vbe=.7;Vcesat=.2;//given
Vled=1.4;Iled=20*10^-3;
//T=1.1RC
R=T/(1.1*C);
disp(R)
Vo=Vcc-2*Vbe-Vcesat;//output of timer
disp(Vo)
Rled=(Vo-Vled)/Iled;
disp(Rled)//this resistance must be in series whit LED
f=1000;D=95;//for an astable timer
C1=.01*10^-6;
R1=%s;R2=%s;
f=1.44/(R1+2*R2)*C;//frequency----------------eq(1)
D=(R1+R2)/(R1+2*R2)//duty cycle---------------eq(2)
R2=.0555*R1;//from eq(2)
//put it in eq(1)
R1=144*10^3/(1+2*.0555);
disp(R1)
R2=.0555*R1;
disp(R2)
```

Scilab code Exa 8.6 Monostable multivibrator

```
//chapter 8
//example 8.6
//page 302
T=5*10^-3;
C=.1*10^-6;
//T=1.1RC
R=T/(1.1*C);
disp(R)//value of R should be less than 100k as
```

```
obtain above
```

Scilab code Exa 8.7 555 based square wave generater

```
//chapter8
//example8.7
//page 303
f=1000;
T=1/f
Td=T/2
C=.1*10^-6;
//Td=.69R2C
R2=Td/(.69*C);
disp(R2)
R1=R2//for square wave R1=R2
```

Chapter 9

Active filter

Scilab code Exa 9.1 cut off frequency

```
//chapter 9
//example 9.1
//page 323
R=10*10^3;C=.001*10^-6;
Rf=100*10^3;R1=10*10^3;
fc=1/(2*3.14*R*C);//cut off frequency
disp(fc)
Ao=1+(Rf/R1);//pass band voltage gain
disp(Ao)//pass band voltage gain
```

Scilab code Exa 9.2 first order low pass filter

```
//chapter 9
//example 9.2
//page 324
Ao=2;fc=10*10^3;
Rf=10*10^3;//let choose
//Ao=1+(RF/R1)
```

```
R1=Rf/(Ao-1);
disp(R1)
C=.001*10^-6;
R=1/(2*3.14*fc*C);
disp(R)
```

Scilab code Exa 9.3 second order low pass filter

```
//chapter9
//example9.3
//page327
fc=1000;
C2=.005*10^-6;R1=33*10^3;//let assume
C3=C2;C=C2;
R3=1/(2*3.14*fc*C);
disp(R3)
R2=R3
Rf=.586*R1;
disp(Rf)
```

Scilab code Exa 9.4 cutoff frequency and pass band voltage gain

```
//chapter9
//example9.4
//page327
R1=12*10^3;Rf=7*10^3;R2=33*10^3;R3=33*10^3;R
    =33*10^3;
C3=.002*10^-6;C2=.002*10^-6;C=.002*10^-6;
fc=1/2*3.14*sqrt(R2*R3*C2*C3);
disp(fc)//cut off frequency
Af=1+(Rf/R1);//passband voltage gain(Avf)
disp(Af)
```

Scilab code Exa 9.5 butterworth low pass filter

```
//chapter9
//example9.5
//page333
fc=1.5*10^3;
Ri=1;
x=sqrt(2);
Rf=(2-x);//for equal component model
disp(Rf)
Af=1+(Rf/Ri);//pass band gain of equal component
    model
Wc=2*3.14*fc;
C=1;
R=1/(Wc*C);
disp(R)
R1=R;R2=R;
R1=R*10^7;R2=R*10^7;//to increase R reasonable value
     we multiply R1 nad R2 by 10^7
disp(R1,R2)
C1=C*10^-7;C2=C*10^-7;//in order to keep value of fc
     unchanged we have to decrease C1 and C2 by same
    factor
disp(C1,C2)
```

Scilab code Exa 9.6 second order butterworth filter

```
//chapter 9
//example9.6
//page 335
fc=1.5*10^3;
x=1.414;//damping factor
```

```
C1=2/x;
disp(C1)
C2=x/2;
disp(C2)
R1=1;R2=1;
Rf=2;
Wc=1;
Wc=2*3.14*fc;
disp(Wc)
R=R1/Wc;//to keep C1 nad C2 unchanged
disp(R)
Rf=2*R
R1=R*10^7;R2=R*10^7;//for maiking filter for
    practical use
disp(R1,R2)
C1=C1*10^-7;C2=C2*10^-7;//to fc remain unchanged
disp(C1,C2)
```

Chapter 10

Voltage regulator

Scilab code Exa 10.1 regulated dc supply

```
//chapter 10
//example 10.1
//page 345
Vnl=12;
Vfl=11.6;
Ilmax=100*10^-3;
LR=Vnl-Vfl;//load regulation
disp(LR)
percentage=((Vnl-Vfl)/Vfl)*100//% LOAD REGULATION
Vout=LR;
Ro=Vout/Ilmax;//output resistance
disp(Ro)
```

Scilab code Exa 10.2 rms value of ripple

```
//chapter10
//example 10.2
//page347
```

```
RF=.1;//ripple factor
Vldc=10;
//ripple factor=Vrms/Vldc
Vrms=Vldc*RF;
disp(Vrms)
Vp_p=2*sqrt(2)*Vrms;//peak to peak ripple
disp(Vp_p)//volts
```

Scilab code Exa 10.3 series regulator circuit

```
//chapter 10
//example 10.3
//page349
V_=6;Vz=6;//potential at inverting(-) input is equal
    to vitual
Vr2=Vz;
Vin=30;
Rl=200;
R2=5*10^3;
R1=0;//for minimum Vout
Voutmin=((R1+R2)/R2)*Vz;//minimum output voltage
disp(Voutmin)//minimum voltage
R1=10*10^3;//for maximum output voltage
Voutmax=((R1+R2)/R2)*Vz;
disp(Voutmax)//maximum output voltage
disp(Voutmax,Voutmin)//range when potentiometer
   change from 0 to 10k
Vce=Vin-Voutmax;//when R1=10k and Vout=18
disp(Vce)
Ic=Voutmax/Rl;
disp(Ic)
Pd=Vce*Ic;//power
disp(Pd)//watt
```

Scilab code Exa 10.4 output voltage for regulator

```
//chapter 10
//example 10.4
//page 350 figure 10.9
Vz=5;
V_=5;
R2=15;R3=15;
//V_ across R3
Vout=((R2+R3)/R3)*(V_)//voltage across R3
disp(Vout)
```

Scilab code Exa 10.5 power rating

```
//chapter 10
// example 10.5
// page 351
R1=20
Vin=12;
Vout=0;//worst case  for masimum power across R1
VR1=Vin-Vout;
disp(VR1)
PR1=VR1^2/R1;
disp(PR1)//watt
```

Scilab code Exa 10.6 adjustable voltage

```
//chapter 10
//eaxmple 10.6
```

```
//page 354
Iq=4.3*10^-3;
R2=100;
Vout=7;//for maximum output voltage
Vr=5;//for R2 is maximum
//Vout=Vout(1+R2/R1)+Iq*R2
R1=100/(((Vout-Iq*R2)/Vr)-1)
```

Scilab code Exa 10.10 min and max output voltage for regulator

```
//chapter 10
//example 10.10
//page 357
Vref=-1.25;
Iadj=50*10^-6;
R1=240;
R2min=0;//to find minimum output voltage correspond
    to R2min=0
Voutmin=Vref*(1+(R2min/R1))+Iadj*R2min;
disp(Voutmin)
R2max=5*10^3;//for maximum output voltage
Voutmax=Vref*(1+(R2max/R1))+Iadj*R2max;
disp(Voutmax)//volts
```

Scilab code Exa 10.11 voltage IC 723

```
//chapter10
//example 10.11
//page 10.11
Vo=5;Io=50*10^-3;
Isc=75*10^-3;Vin=15;
Vsense=.6;Vref=7;
I=1*10^-3;//current through R1 and R2
```

```
R2=Vo/I;
disp(R2)
VR1=Vref-Vo;//voltage across R1
disp(VR1)
R1=VR1/I;
disp(R1)
R3=R1*R2/(R1+R2);//R3=R1||R2
disp(R3)
Rsc=Vsense/Isc;
disp(Rsc)
C1=7.4*10^-6/10;
disp(R1,R2,R3,Rsc,C1)//component value
```

Scilab code Exa 10.12 power dissipation in regulator

```
//chapter 10
//example 10.12
//page 372
Vref=7;Vout=5;Vin=15;
Il=1*10^-3;Isc=1.5;Vsense=.65;
Imax=150*10^-3;//Imax of IC-723 is 150mA
R1=(Vref-Vout)/Il;
disp(R1)
R2=Vout/Il;
disp(R2)
R3=(R1*R2)/(R1+R2);
disp(R3)
Rsc=Vsense/Isc;
disp(Rsc)
Bmin=Il/Imax
Pd=(Vin-Vout)*Isc
Icmax=2*Isc;//Maximum collector current
disp(Icmax)
Vout=0;//maximum collector to emitter voltage can be
    calculated as under the voltage across Q will
```

```
   maximum when the load is short circuited
Vcemax=Vin-Vout;
disp(Vcemax)
```

Scilab code Exa 10.13 design a regulated power supply

```
//chapter 10
//example 10.13
//page 373
Vref=7;Vsense=.65;
Voutmin=9;Voutmax=12; I1=.5;Imax=150*10^-3;
R2=10*10^3;//let assume
//(R1+R2)/R2=Vout/Vref------------------------eq(1)
R1min=2*R2/7;
disp(R1min)
Voutmax=12
R1max=5*R2/7;//using eq (1)
disp(R1max)
Rsc=Vsense/Il;
disp(Rsc)
R3=(R1max*R2)/(R1max+R2)
Bmin=Il/Imax;
disp(Bmin)
```

Scilab code Exa 10.14 current source using IC 7805

```
//chapter 10
//example 10.14
//page 376
Rl=10;Iq=4.3*10^-3;
Vr=5;Il=.5;
// Il=Vr/R+Iq
R=Vr/(Il-Iq);
```

```
disp(R)
power=(Il^2)*R;//wattage of reisstor
disp(power)
Vout=Vr+Il*R;//output voltage with respect to ground
disp(Vout)
Vd=2;//minimum voltage drop across IC 7805 which is
    called as drop out voltage is 2V
Vin=Vout+Vd;
disp(Vin)
```

Chapter 11

Phase locked loop

Scilab code Exa 11.1 free running frequency lock range capture range

```
// chapter 11
// example 11.1
//page 394
Rt=10*10^3;Ct=.005*10^-6;C=10*10^-6;
V=20;//in volts
fout=.25/(Ct*Rt);//free running frequency
disp(fout)
fL=(8*fout)/V;//lock range
disp(fL)// it may be -ve or +ve
fc=sqrt(fL/(2*3.14*3.6*1000*C));// capture range
disp(fc)
```

Scilab code Exa 11.2 frequency of oscillator and phase accumulator

```
//chapter 11
//example 11.2
//page 401
foutmax=200*10^3;
```

```
foutmin=4;
n=%s;
fclk=2.2*foutmax;
disp(fclk)//maximum output frequency
//resolution=foutmin=fclk/2^n
2*n==fclk/foutmin;
//n=fclk/(foutmin*2);
//hittrail method n=17
n=17
disp(n)
```

Chapter 12

DA and AD converter

Scilab code Exa 12.1 resolution

```
//chapter 12
//example 12.1
// page 413
n=8;// number of bits
Vofs=2.55;//in volts
R=2^n;//resolution
disp(R)
Resolution=Vofs/(2^8-1);
disp(Resolution)// an input change of 1LSB cause the
    output to change by 10mV
```

Scilab code Exa 12.2 final output voltage

```
//chapter 12
// example 12.2
// page 413
n=4;// 4-bit DAC
Vofs=15;
```

```
inp=0110;
resolution=Vofs/(2^n-1);
disp(resolution)
D=0*2^3+1*2^2+1*2^1+0*2^0;//Decimal value of input
disp(D)
Vout=D*resolution
disp(Vout)
```

Scilab code Exa 12.3 Vofs and Vo

```
// chapter 12
// example 12.3
// page 414
n=8;// 8 bit DAC
R=20*10^-3;//resolution V/LSB
inpt=10000000;
Vofs=R*(2^n-1);
disp(Vofs)
D=1*2^7+0*2^6+0*2^5+0*2^4+0*2^3+0*2^2+0*2^1+0*2^0;
disp(D)
Vout=R*D;//output voltage
disp(Vout)
```

Scilab code Exa 12.4 step size and analog output

```
//chapter
//example 12.4
// page 414
n=4;// 4-bit R-2R ladder
Vofs=5;
R=Vofs/(2^n-1);//resolution
disp(R)
D1=1*2^3+0*2^2+0*2^1+0*2^0;//for input 1000
```

```
disp(D1)
Vout1=R*D1;
disp(Vout1)
D2=1*2^3+1*2^2+1*2^1+1*2^0;// for input 1111
Vout2=R*D2;
disp(Vout2)
```

Scilab code Exa 12.5 full scale output

```
//chapter 12
//example 12.5
// page 414
n=12;//12-bit DAC
R=8*10^-3;// step size
Vofs=R*(2^n-1);
disp(Vofs)
RESpercentage=(R/Vofs)*100
D
  =0*2^11+1*2^10+0*2^9+1*2^8+0*2^7+1*2^6+1*2^5+0*2^4+1*2^3+1*2^2+0*
  // decimal value of 010101101101
disp(D)
Vout=R*D;
disp(Vout)
```

Scilab code Exa 12.6 value of resistor and reference

```
//chapter 12
//example 12.6
//page 419
Vr=10;//let suppose
n=4;//4-bit R/2R ladder
Res=.5;// given Resolution
//Resolution=(1/2^n*Vr/R)*Rf
```

```
Rf=10;//let choose
R=(1/2^n)*(Vr/Res)*Rf;
disp(R)
```

Scilab code Exa 12.7 resolution and digital output

```
//chapter 12.7
// example 12.7
//page 425
n=8;//8 bit ADC
Vi=5.1;// when all output is 1
Res1=2^n;
Res2=Vi/(2^n-1);//resolution
disp(Res1,Res2)
vi=1.28;
D=vi/Res2;
disp(D)// digital output
B=(01000000)// binary equivalent of 64
```

Scilab code Exa 12.8 quantizing error

```
//chapter 12
// example 12.8
//page 426
n=12;// 12-bit ADC
Vi=4.095;//input voltage
Qe=Vi/((2^n-1)*2);// quqntizing error
disp(Qe)
```

Scilab code Exa 12.9 calculate t2

```
//chapter 12
// example 12.9
// page 428
t1=83.33;
Vr=100*10^-3;//reference voltage
Vi=100*10^-3;
t2=(Vi/Vr)*t1;
disp(t2)
Vi=200*10^-3;
t2=(Vi/Vr)*t1;
disp(t2)//is in msec
```

Scilab code Exa 12.10 digital output

```
//chapter 12
//example 12.10
//page 429
t1=83.33;
Vr=100*10^-3;// reference voltage
Vi=100*10^-3;//input voltage
Cf=12*10^3;//clock frequency
DIGITALVout=Cf*t1*(Vi/Vr)
disp(DIGITALVout)
```

Scilab code Exa 12.11 conversion time

```
//chapter 12
// example 12.11
//page 431
f=1*10^6;
n=8;//8-bit ADC
T=1/f;//time period
Tc=T*(n+1);
```

```
disp(Tc)//conversion time
```

Scilab code Exa 12.12 maximum frequency

```
//chapter 12
//example 12.12
//page 432
Tc=9*10^-6;
n=8;//8-bit ADC
fmax=1/(2*%pi*Tc*2^n);// maximum frequency
disp(fmax)//Hz
```