

Scilab Manual for
Simulation lab / Pulse & Digital Circuits lab /
SEEK Course (Skill for Employability
Enhancement of Knowledge) / DLDMP lab
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Experiment: 1

Digital Logic Gates Design & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

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EX-OR Gate Implementation using Basic Logic Gates

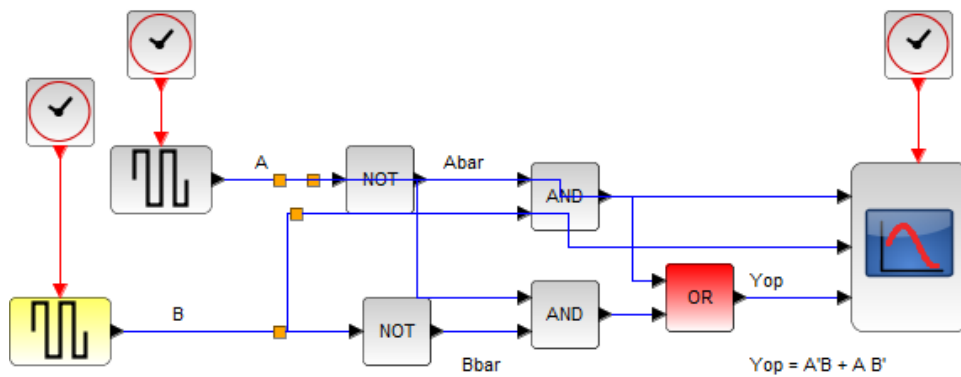


Figure 1.1: XOR gate design using basic logic gates

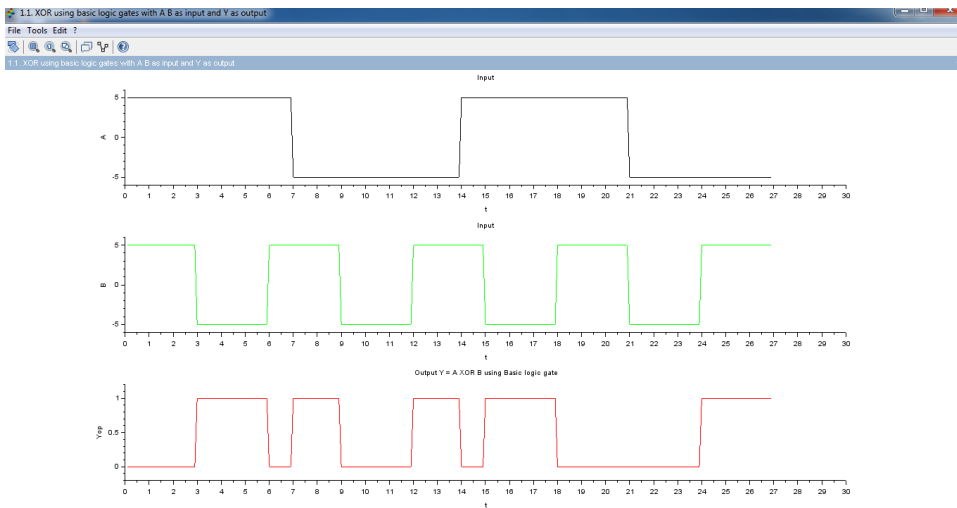


Figure 1.2: XOR gate design using basic logic gates

EX-OR Gate Implementation using Universal Logic Gate NAND only

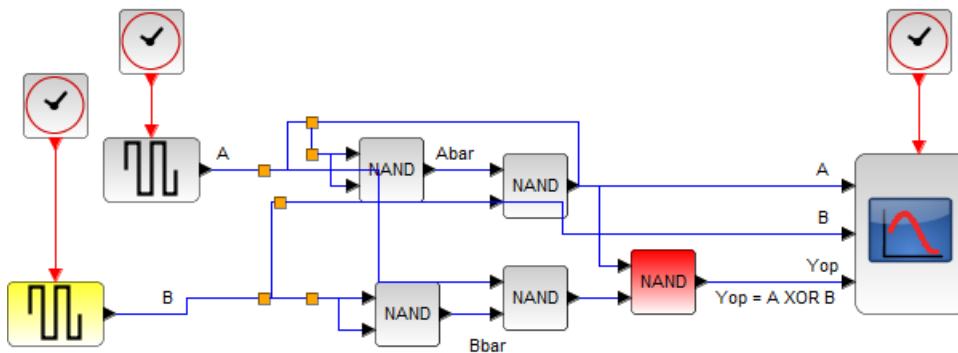


Figure 1.3: XOR gate design using NAND gate

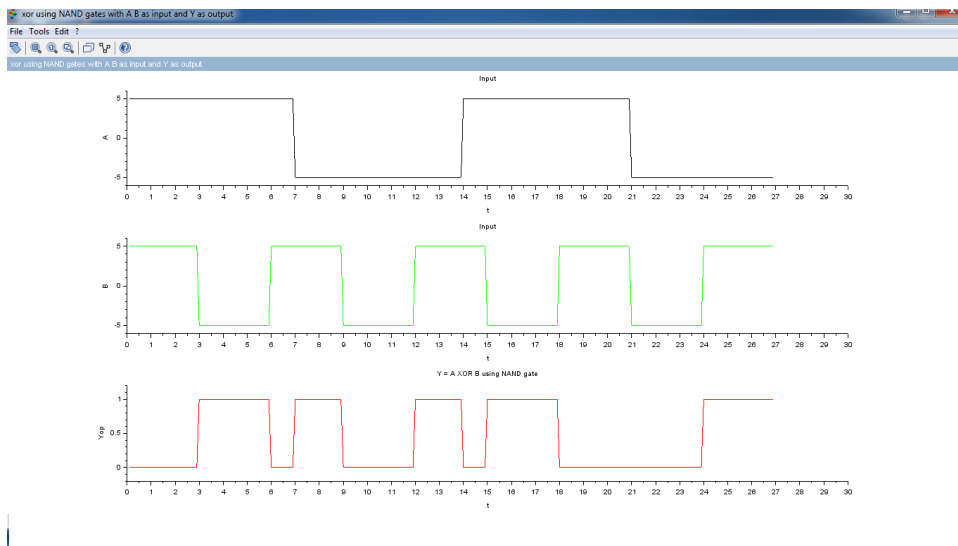


Figure 1.4: XOR gate design using NAND gate

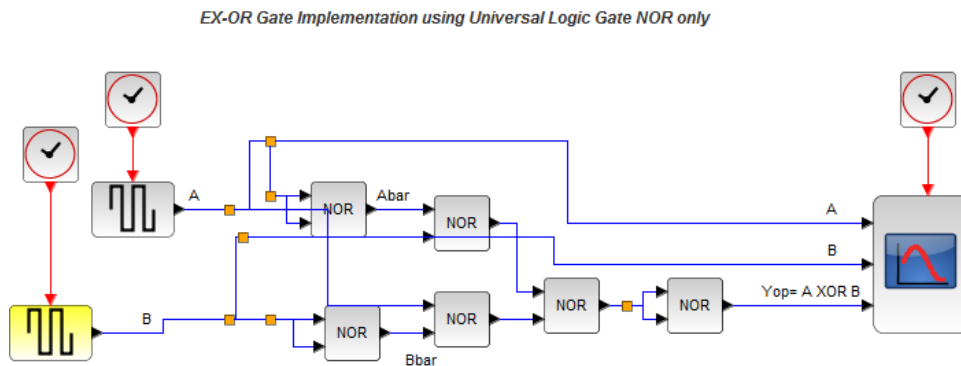


Figure 1.5: XOR gate design using NOR gate

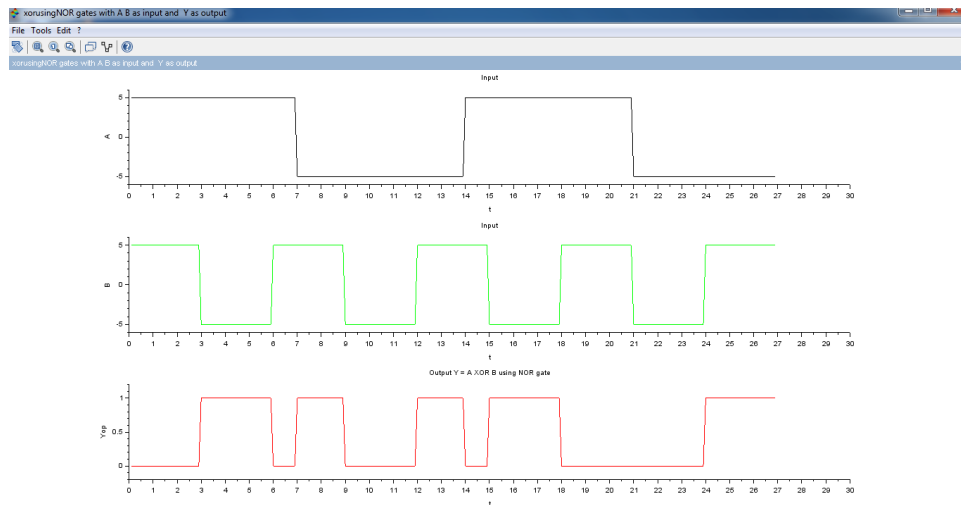


Figure 1.6: XOR gate design using NOR gate

Experiment: 2

Half Adder and Full Adder Design & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

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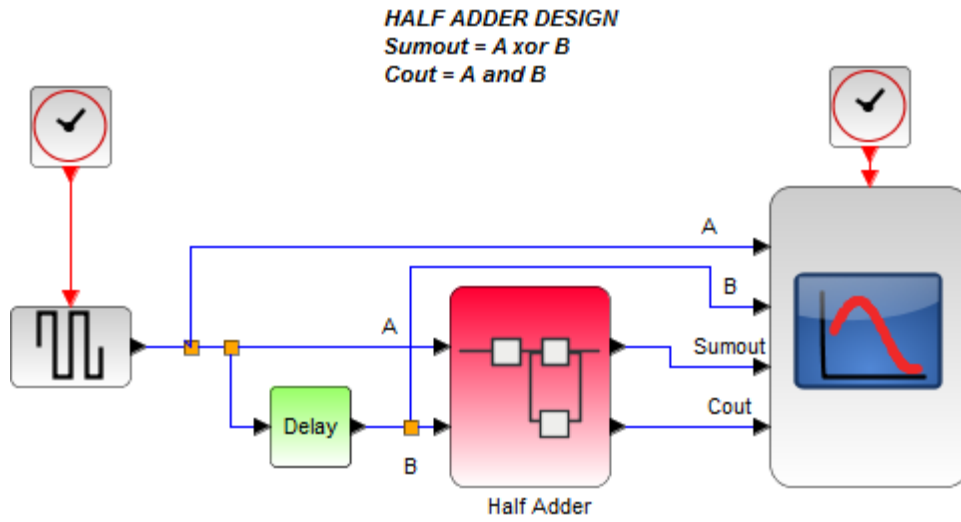


Figure 2.1: Half Adder design

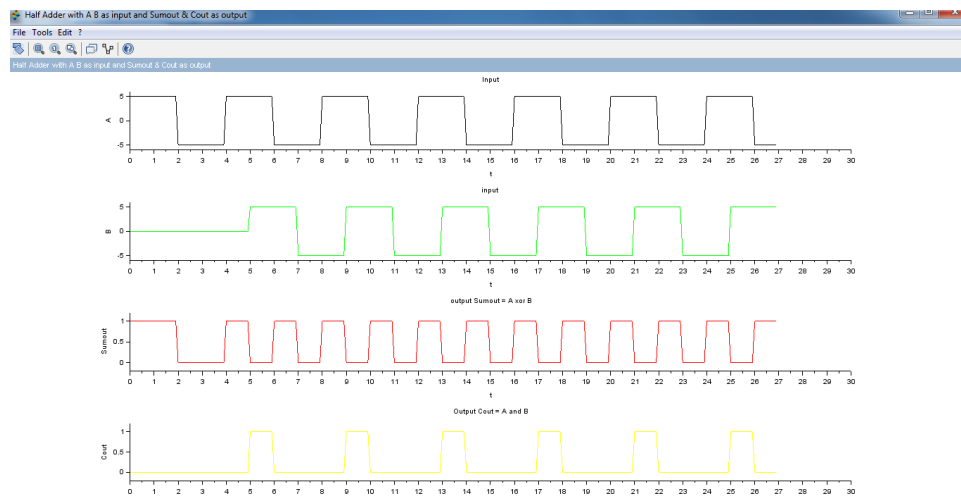
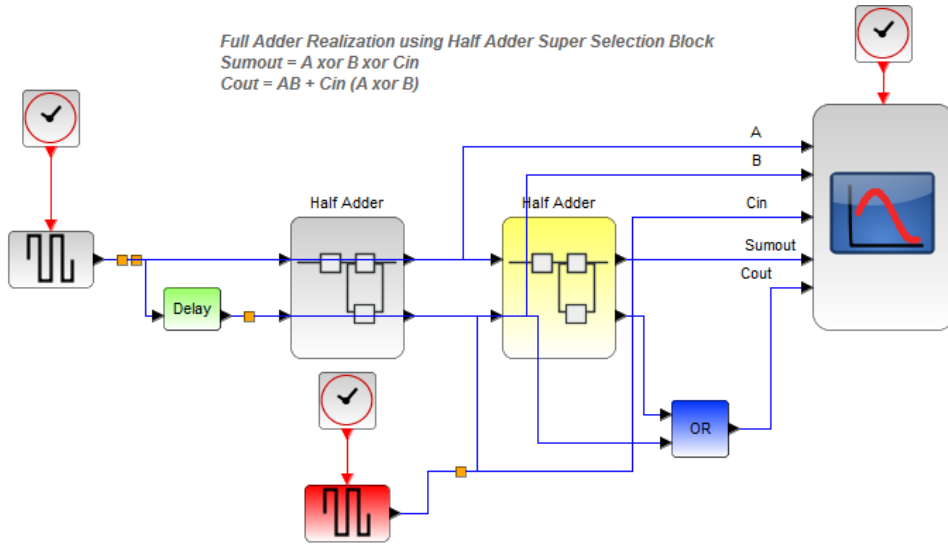


Figure 2.2: Half Adder design



Note : Superselection of superselection not supported in Scilab Xcos.

Figure 2.3: Full Adder Design

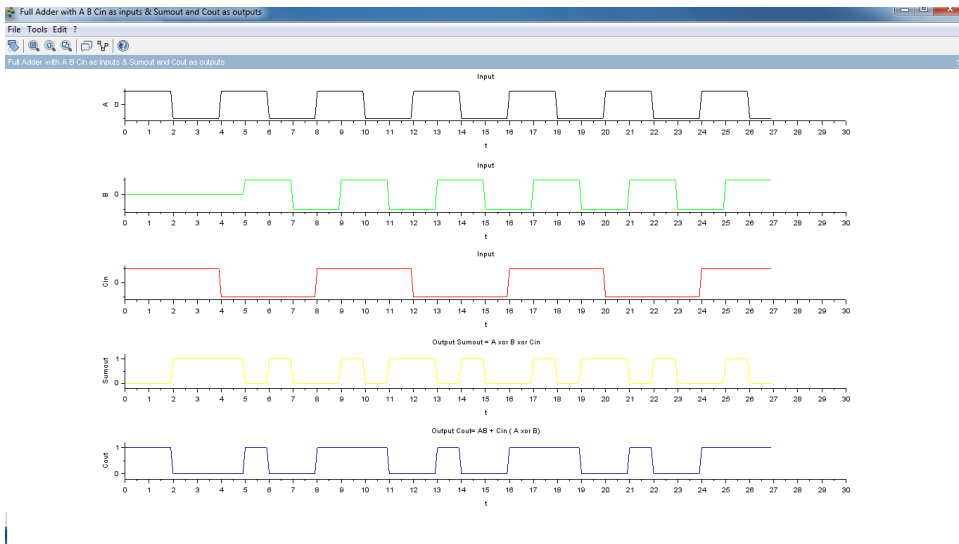


Figure 2.4: Full Adder Design

Experiment: 3

Half Subtractor and Full Subtractor Design & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

This code can be downloaded from the website www.scilab.in

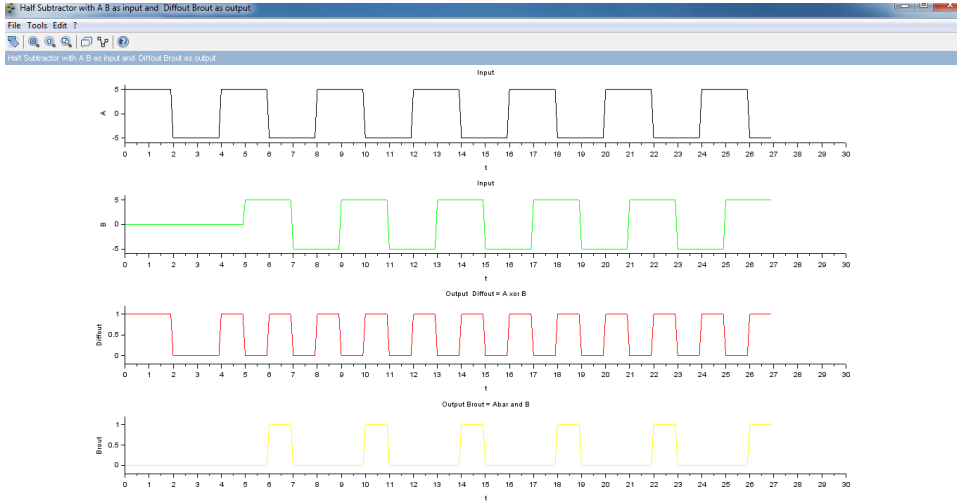


Figure 3.1: Half Subtractor design

Half Subtractor Design
 $Diffout = A \text{ xor } B$
 $BrouT = A' B$

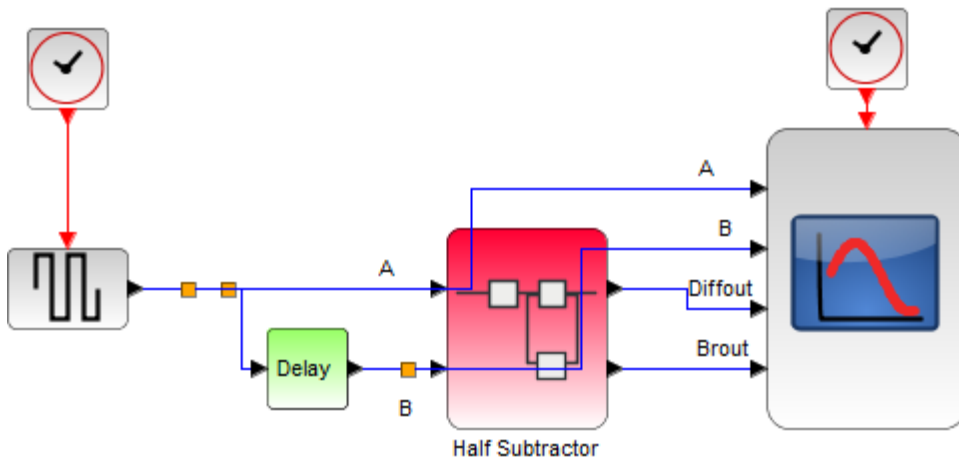
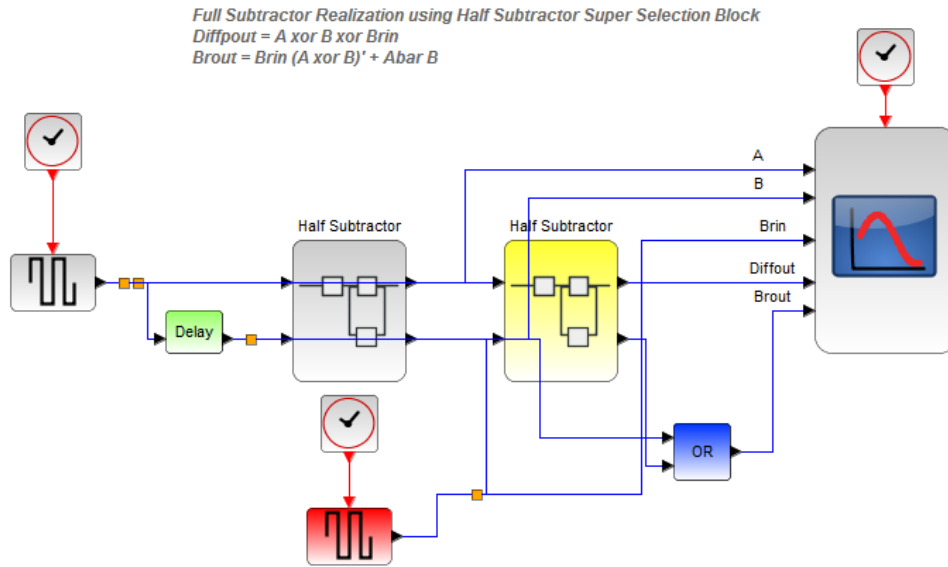


Figure 3.2: Half Subtractor design



Note : Superselection of superselection not supported in Scilab Xcos.

Figure 3.3: Full Subtractor Design



Figure 3.4: Full Subtractor Design

Experiment: 4

4 bit Ripple Carry Adder Design & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

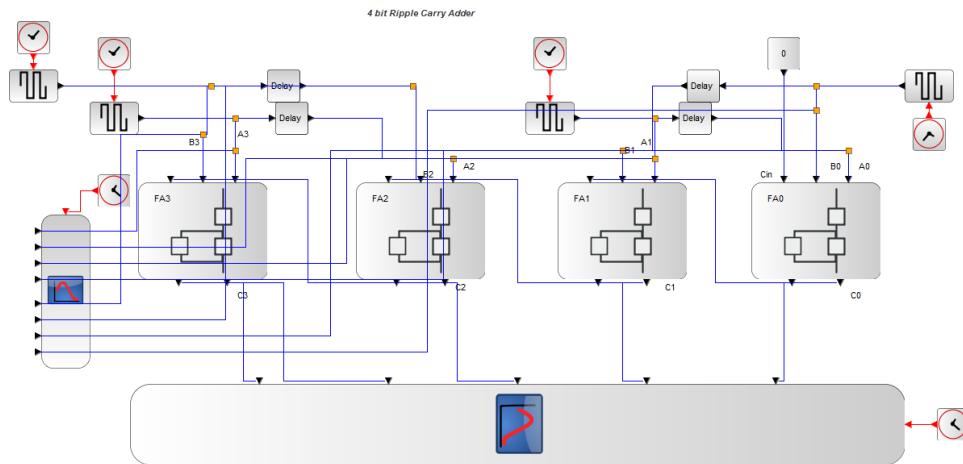


Figure 4.1: Ripple Carry Adder Design

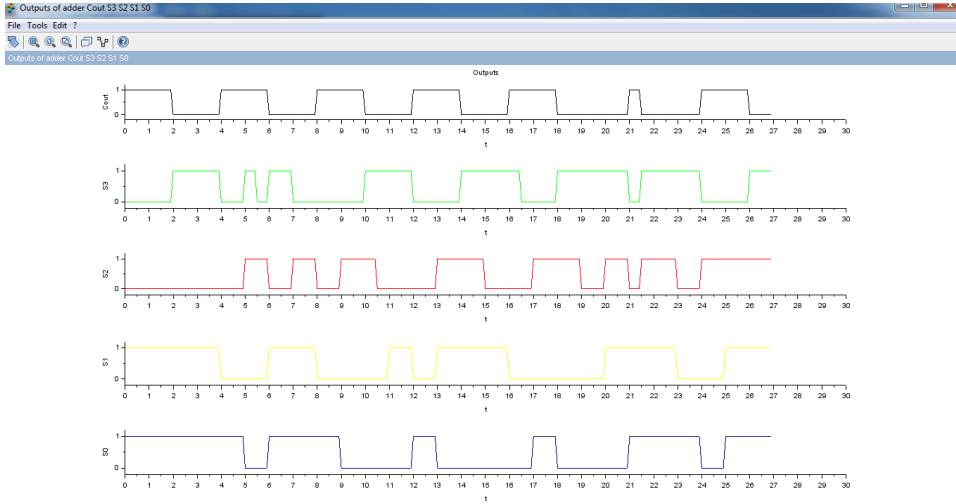


Figure 4.2: Ripple Carry Adder Design

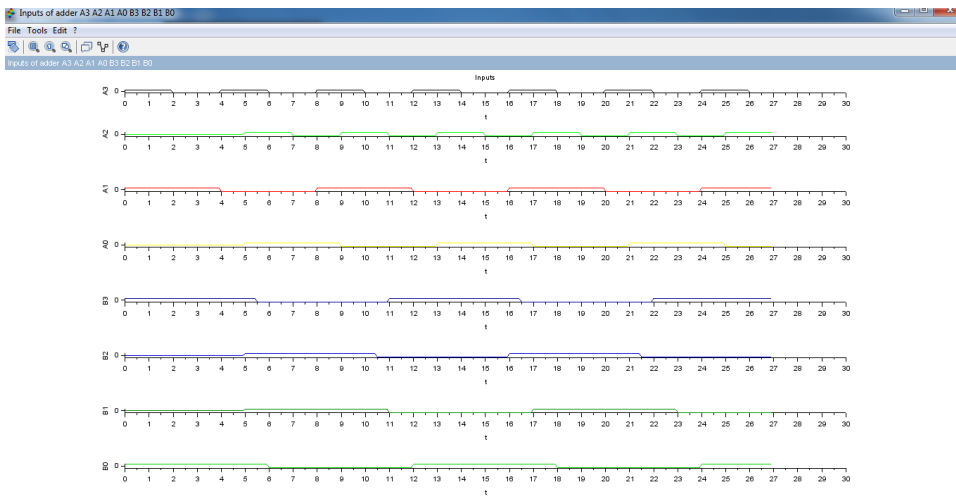


Figure 4.3: Ripple Carry Adder Design

Experiment: 5

BCD Adder Design & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

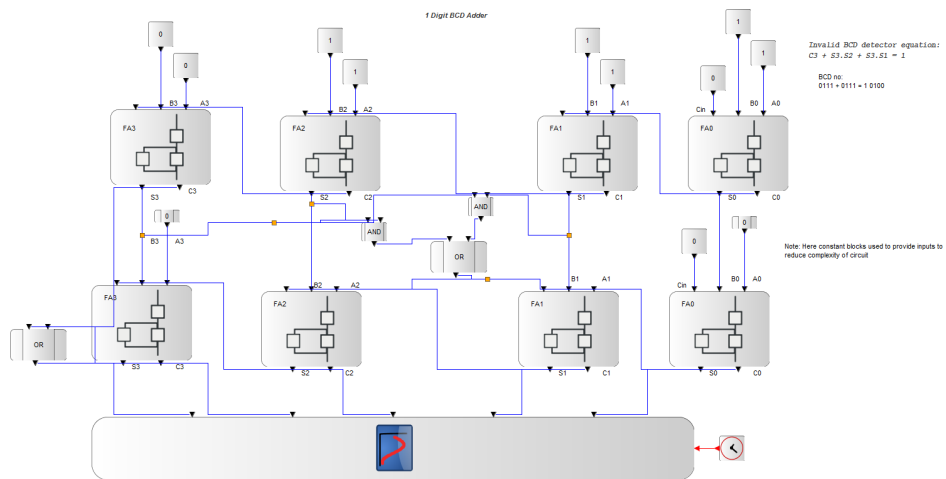


Figure 5.1: BCD Adder Design

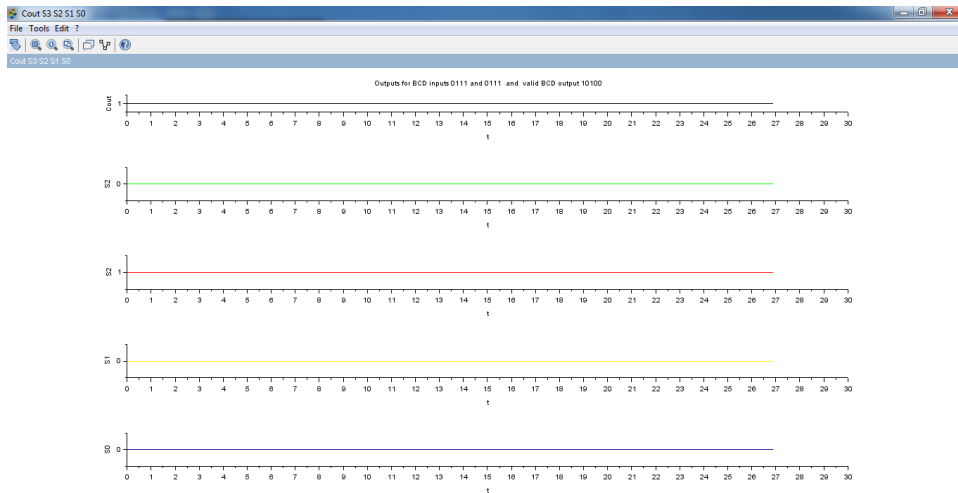


Figure 5.2: BCD Adder Design

Experiment: 6

Multiplexer Design and implementation & its application in Xcos

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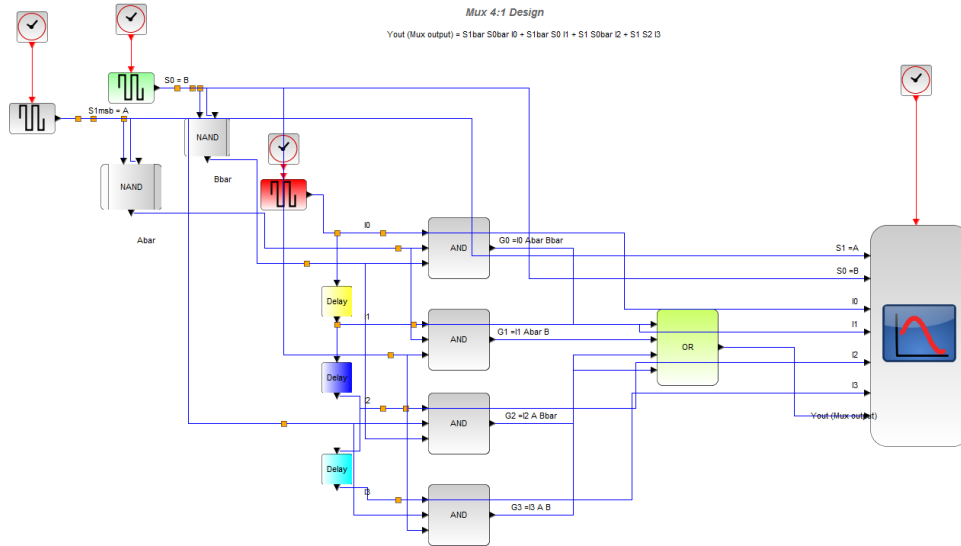


Figure 6.1: Multiplexer 4 to 1 design

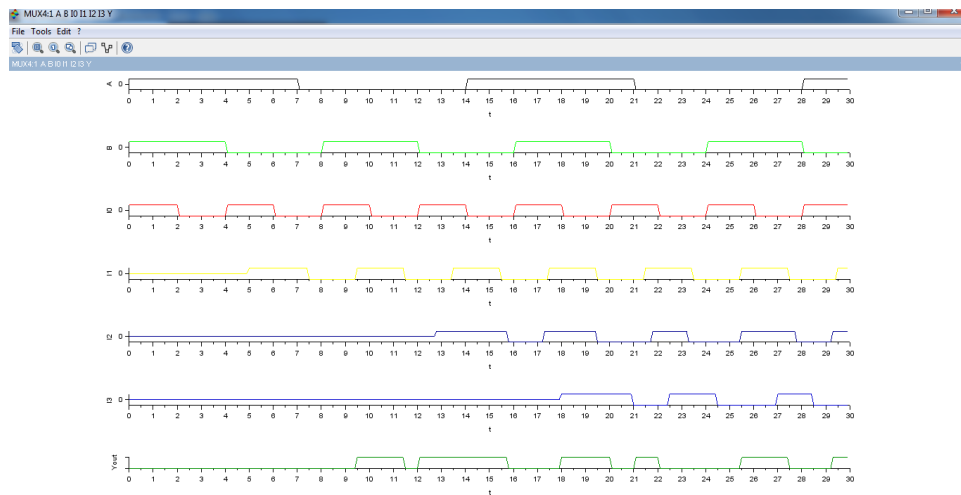


Figure 6.2: Multiplexer 4 to 1 design

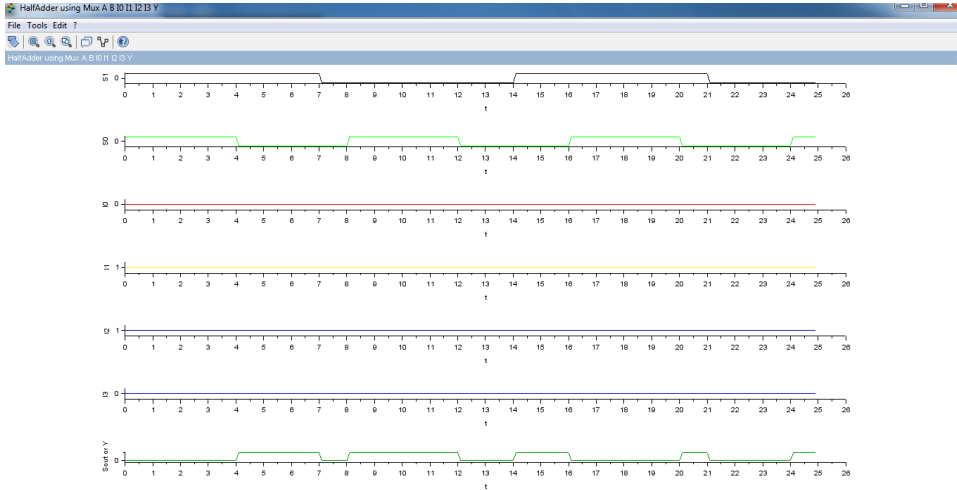


Figure 6.3: Multiplexer Application Half Adder design

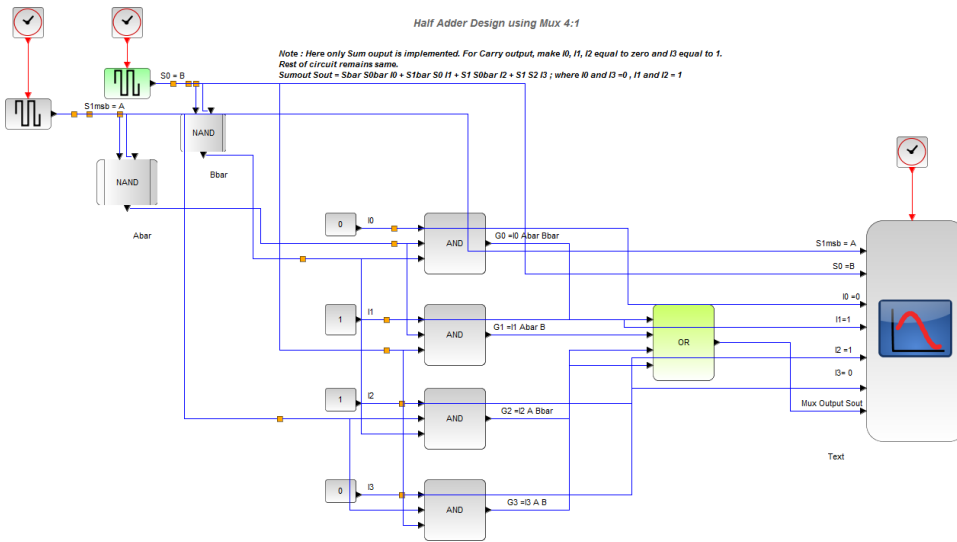


Figure 6.4: Multiplexer Application Half Adder design

Experiment: 7

Demultiplexer Design and implementation & its application in Xcos

This code can be downloaded from the website www.scilab.in

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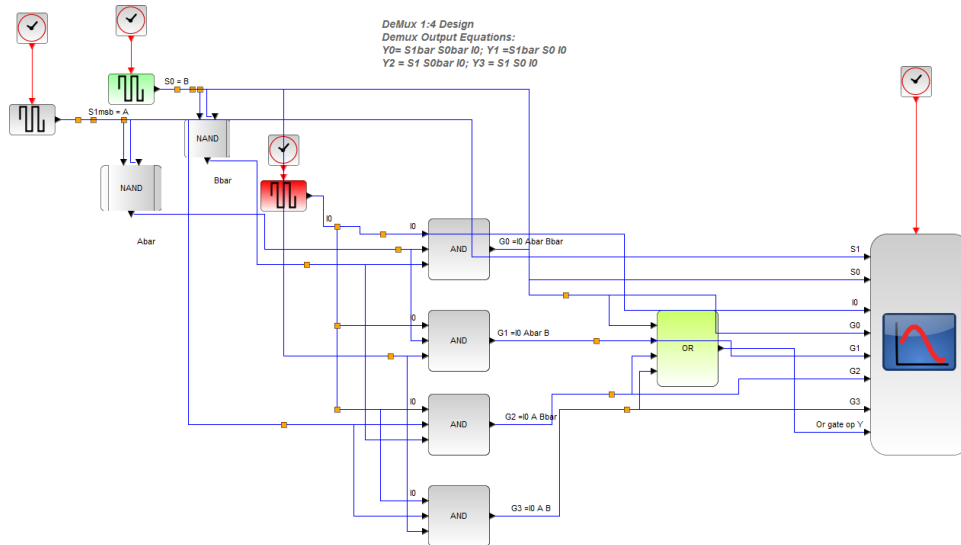


Figure 7.1: Demultiplexer 1 to 4

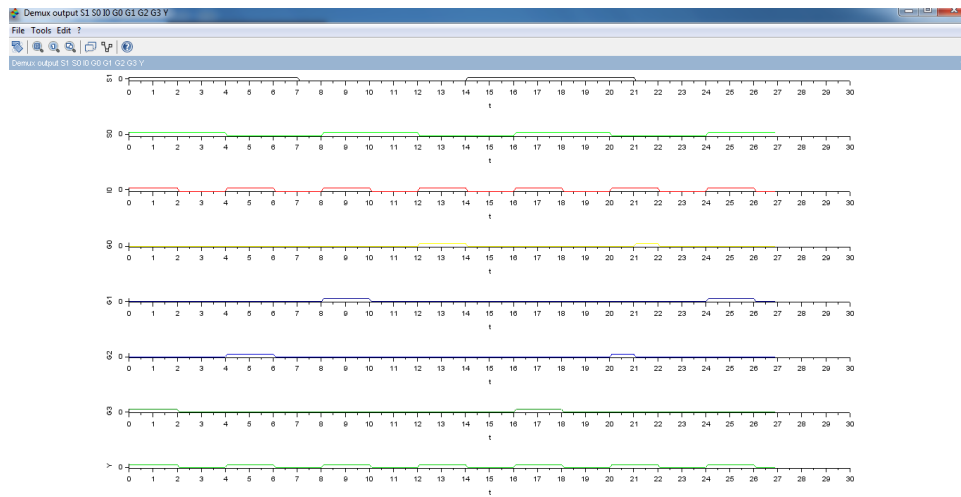


Figure 7.2: Demultiplexer 1 to 4

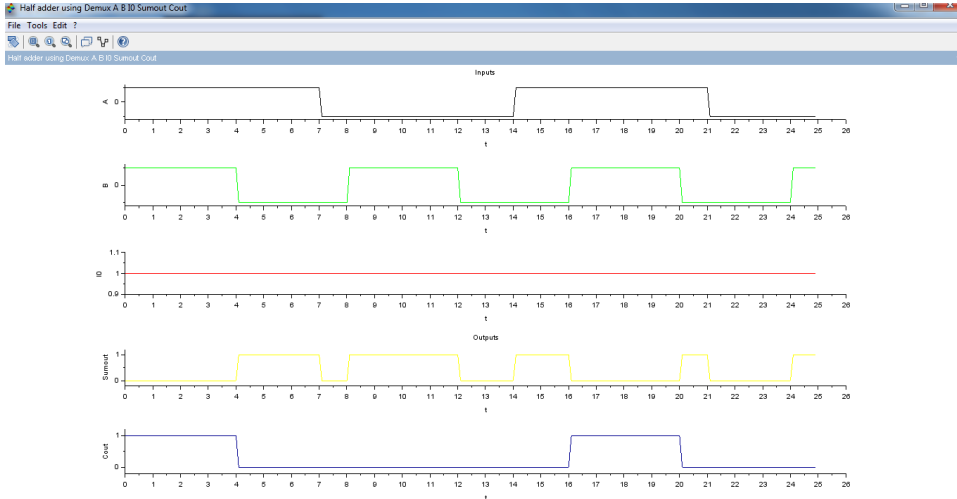


Figure 7.3: Demultiplexer Application Half Adder design

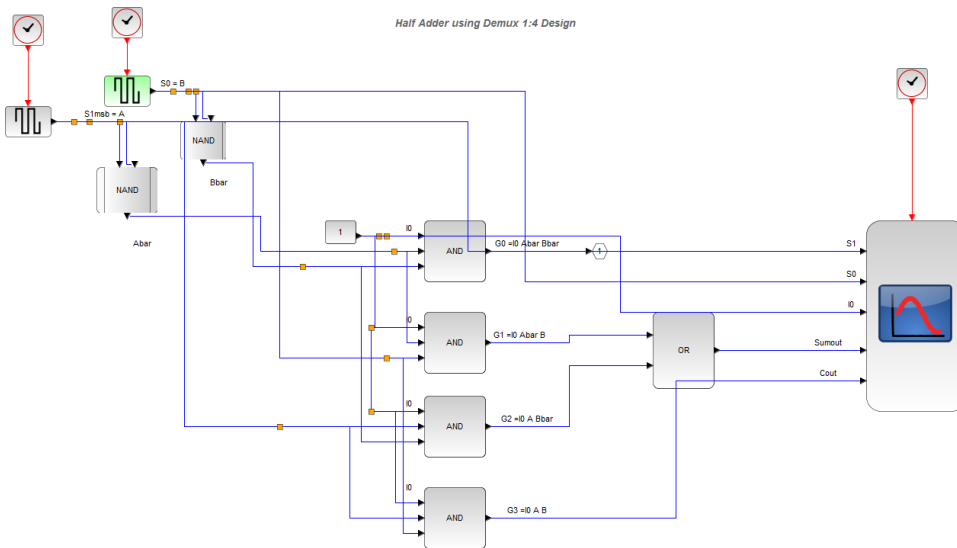


Figure 7.4: Demultiplexer Application Half Adder design

Experiment: 8

Decoder Design and implementation & its application in Xcos

This code can be downloaded from the website www.scilab.in

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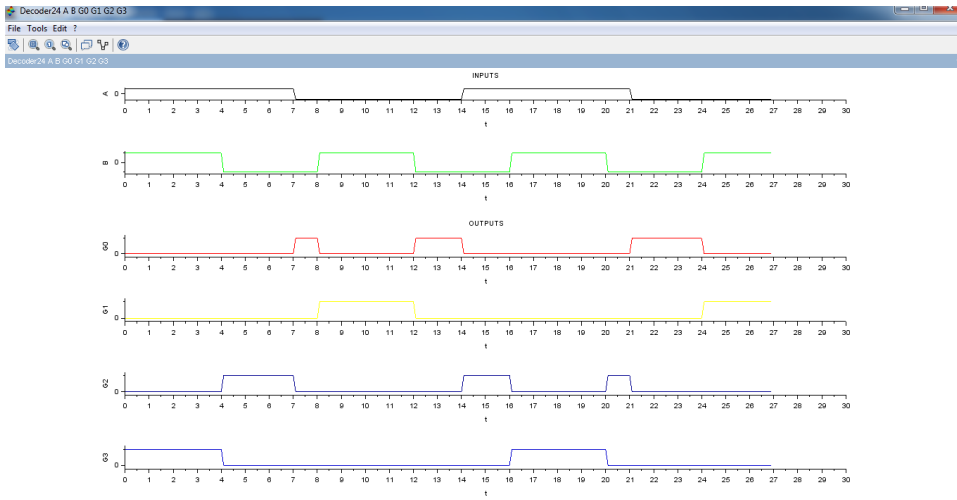


Figure 8.1: Decoder 2 to 4 design

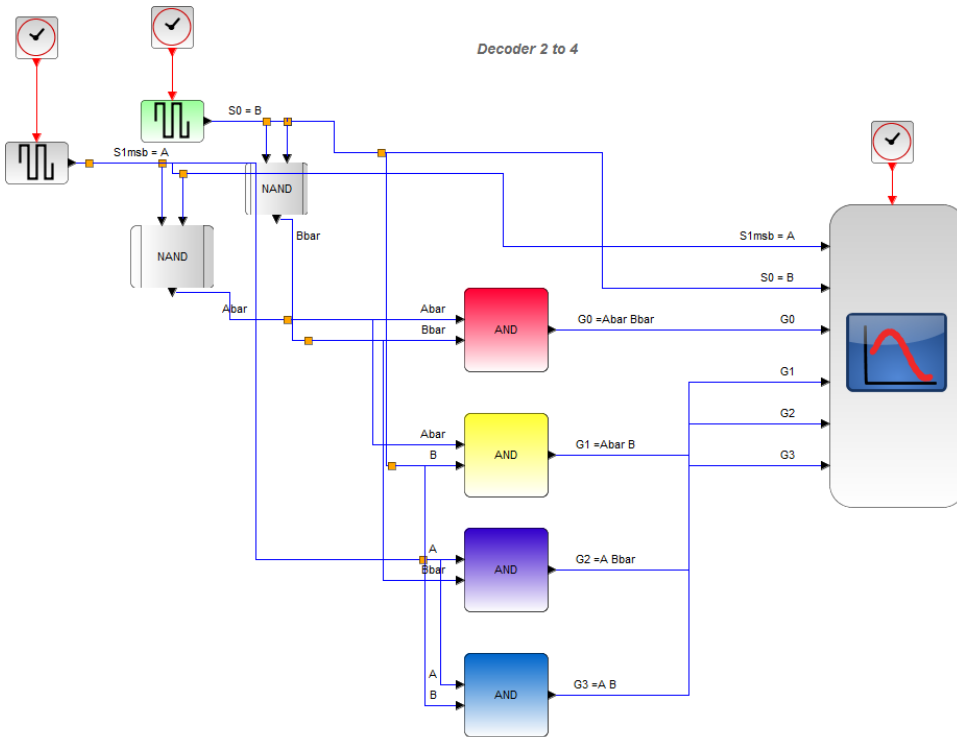


Figure 8.2: Decoder 2 to 4 design

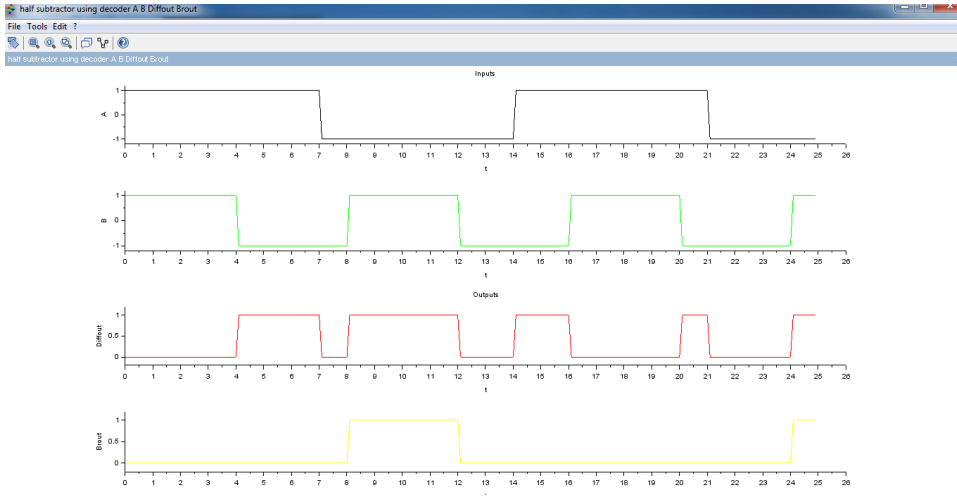


Figure 8.3: Decoder Application Half Subtractor design

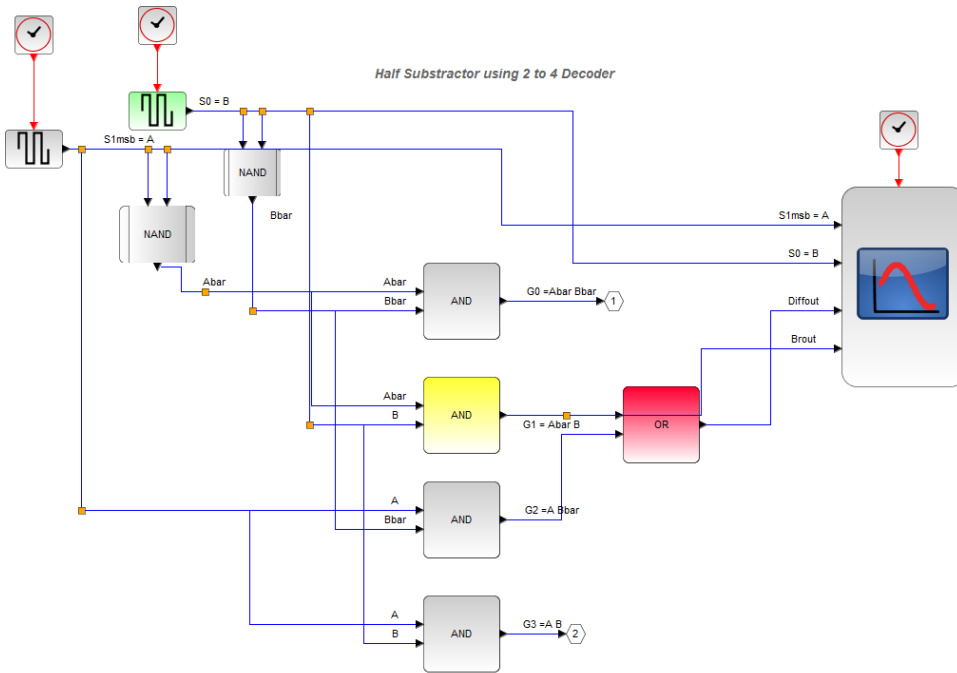


Figure 8.4: Decoder Application Half Subtractor design

Experiment: 9

Flip flop Design & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

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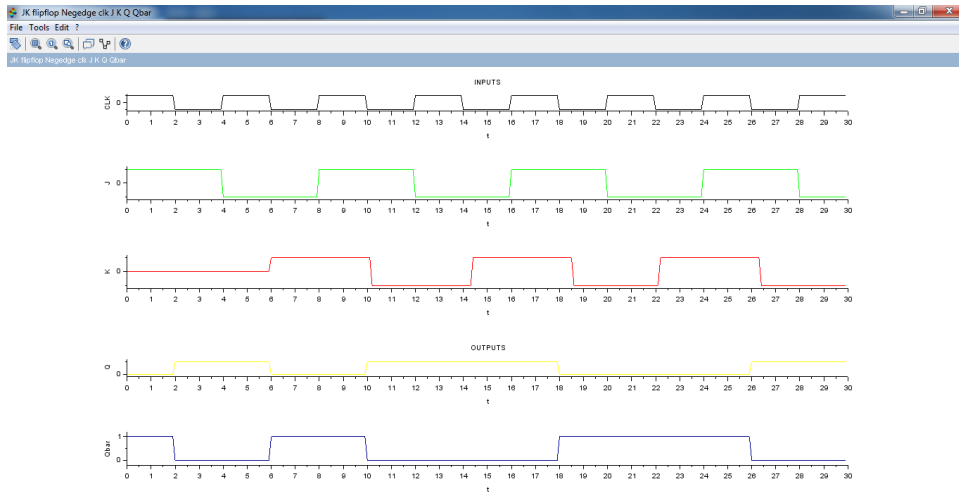


Figure 9.1: JK flip flop

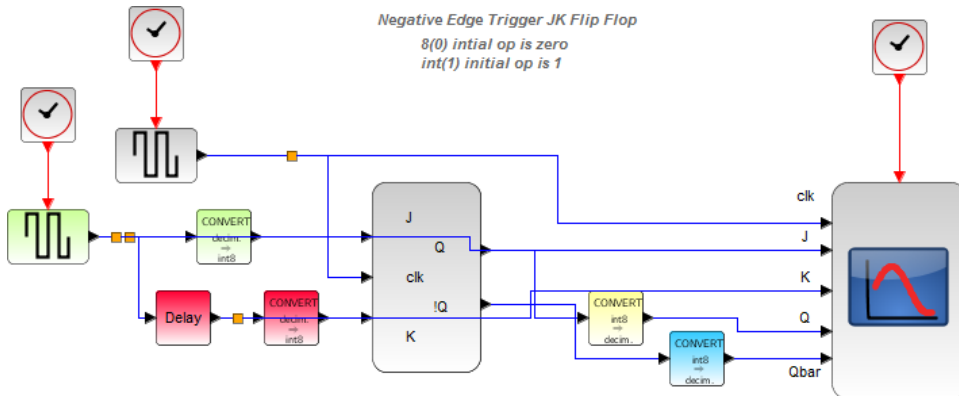


Figure 9.2: JK flip flop

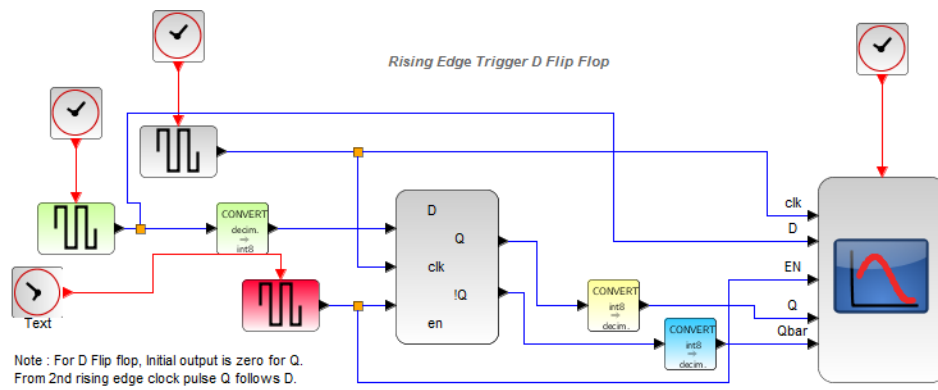


Figure 9.3: D flip flop

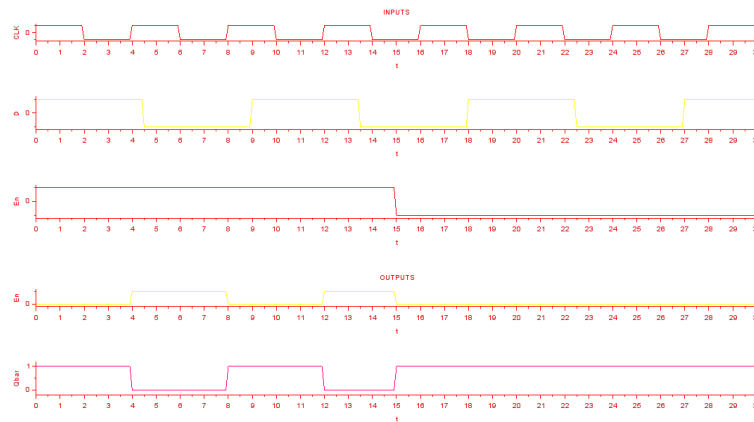


Figure 9.4: D flip flop

Experiment: 10

Asynchronous Counter Design & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

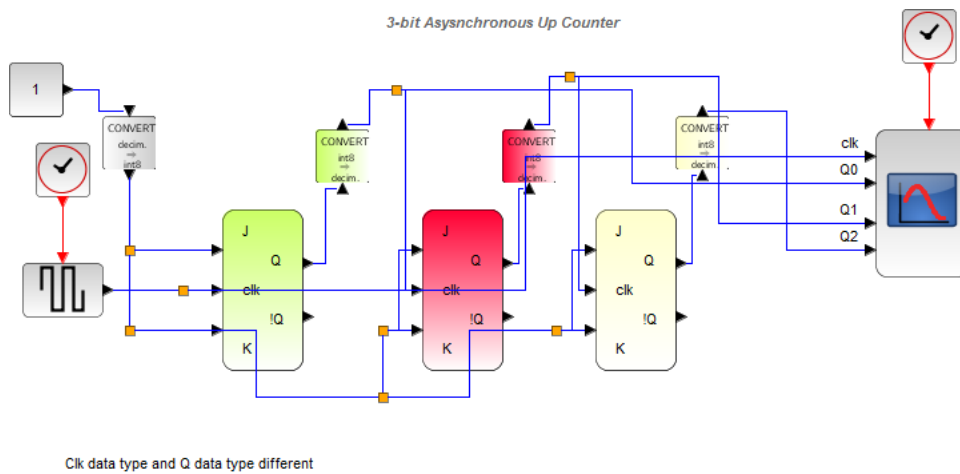


Figure 10.1: Asynchronous 3 bit up counter design

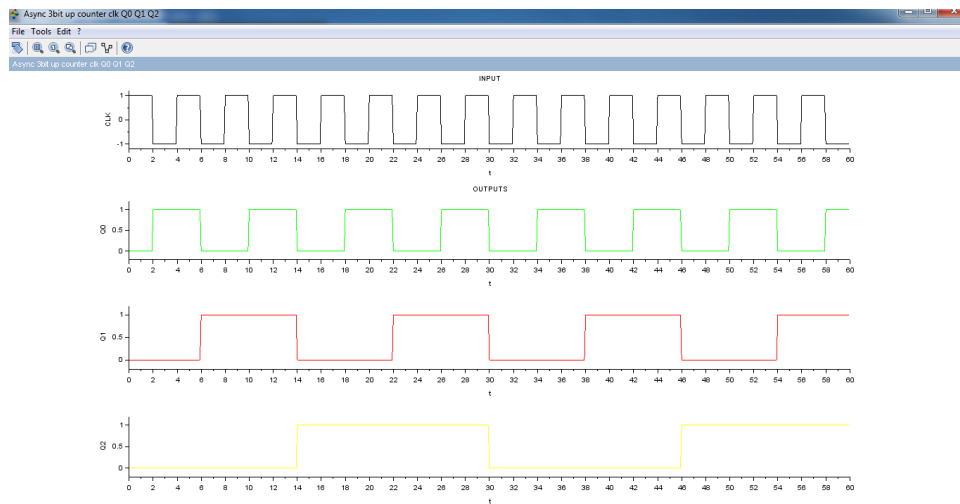


Figure 10.2: Asynchronous 3 bit up counter design

Experiment: 11

Synchronous Counter Design & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

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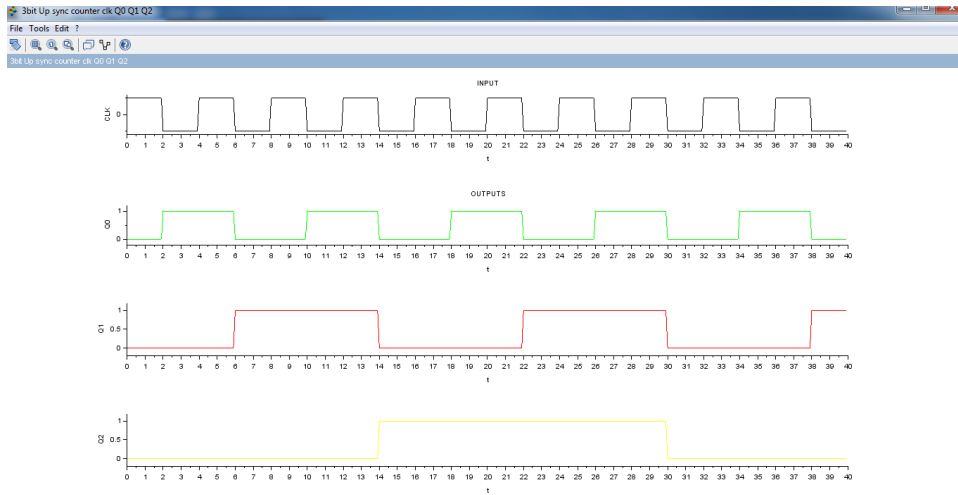


Figure 11.1: Three bit up synchronous counter

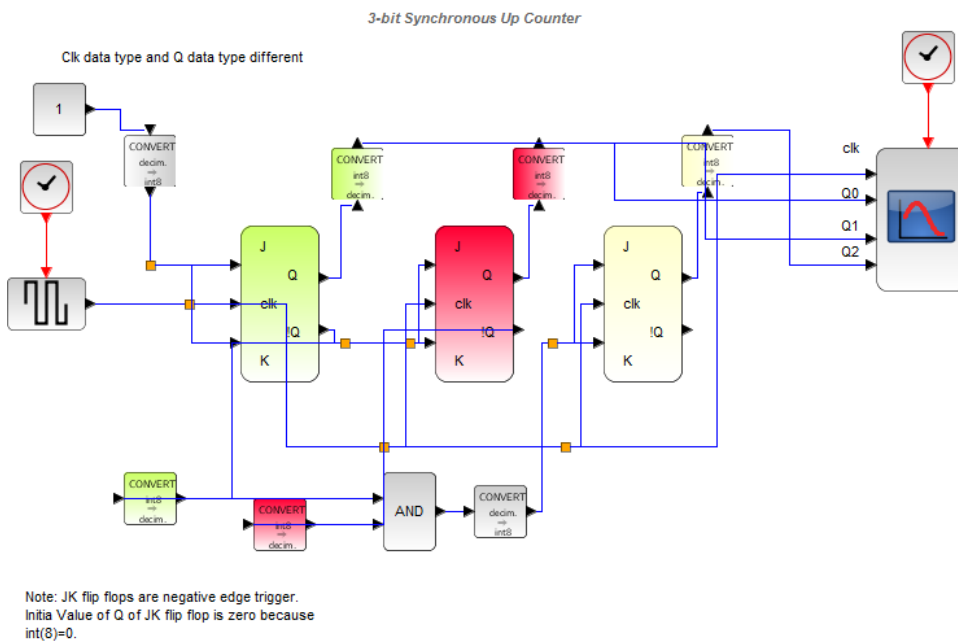


Figure 11.2: Three bit up synchronous counter

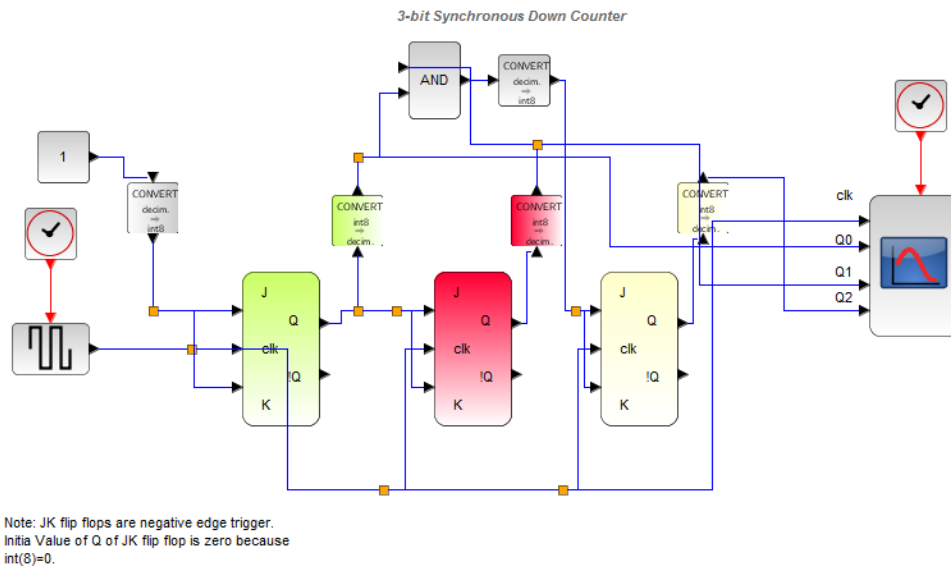


Figure 11.3: Three bit down synchronous counter

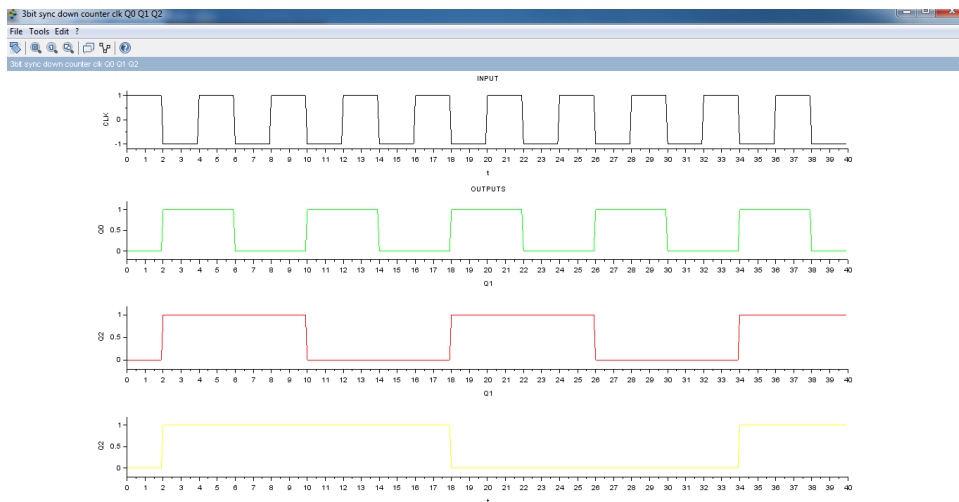


Figure 11.4: Three bit down synchronous counter

Experiment: 12

Code Converter Design (eg.binary to gray code conversion) & Implementation in Xcos

This code can be downloaded from the website www.scilab.in

Code Converter : 4 bit Binary to 4 bit Gray

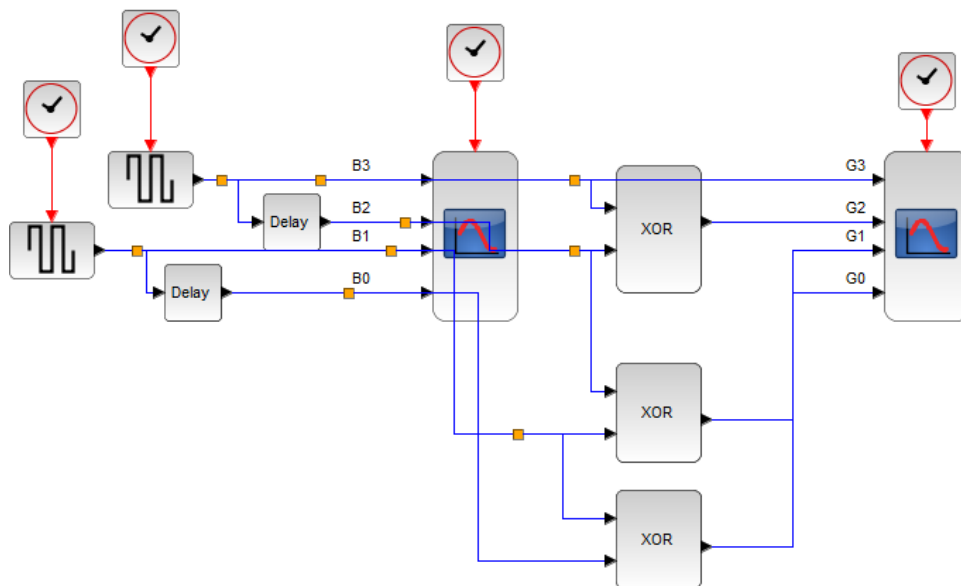


Figure 12.1: Binary to Gray code converter

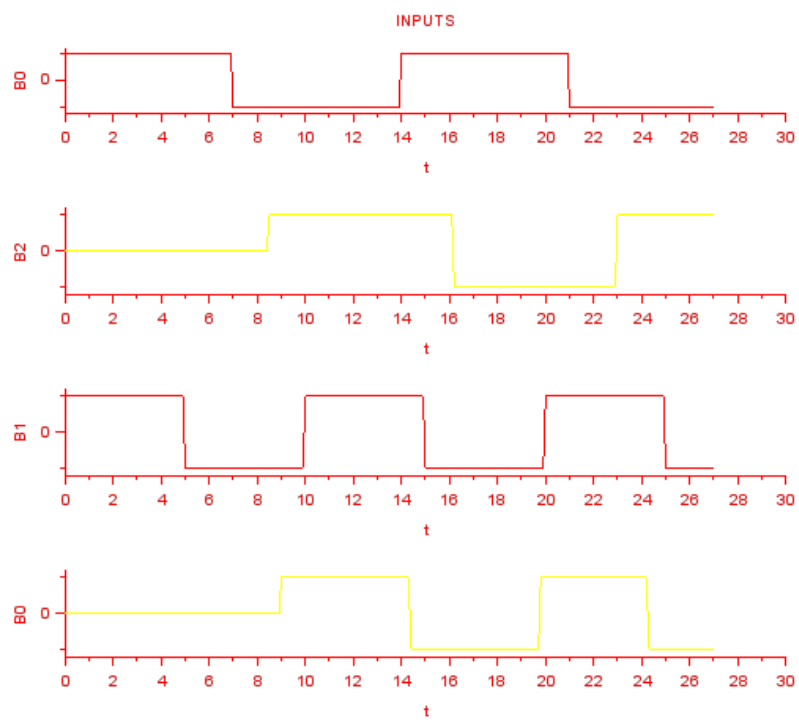


Figure 12.2: Binary to Gray code converter

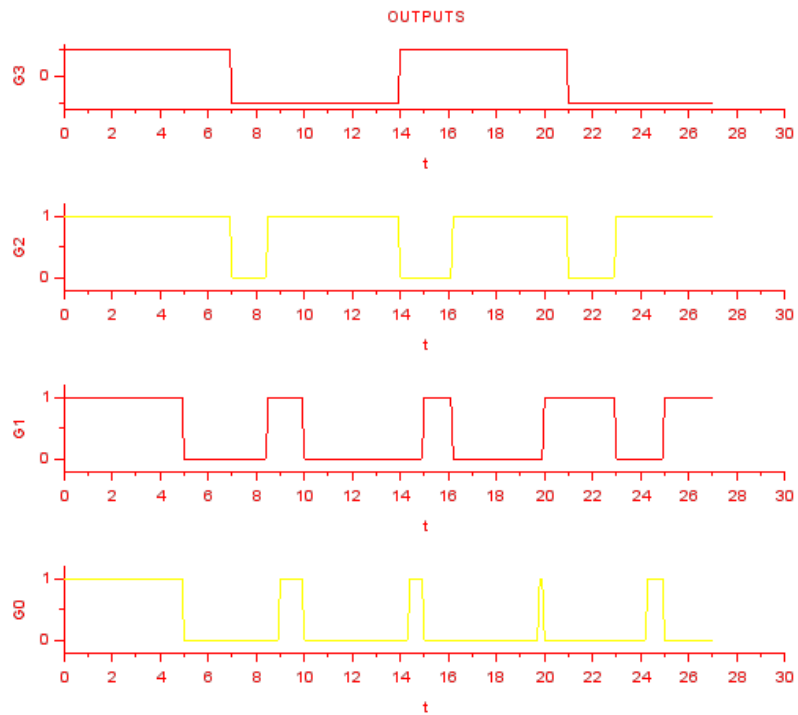


Figure 12.3: Binary to Gray code converter

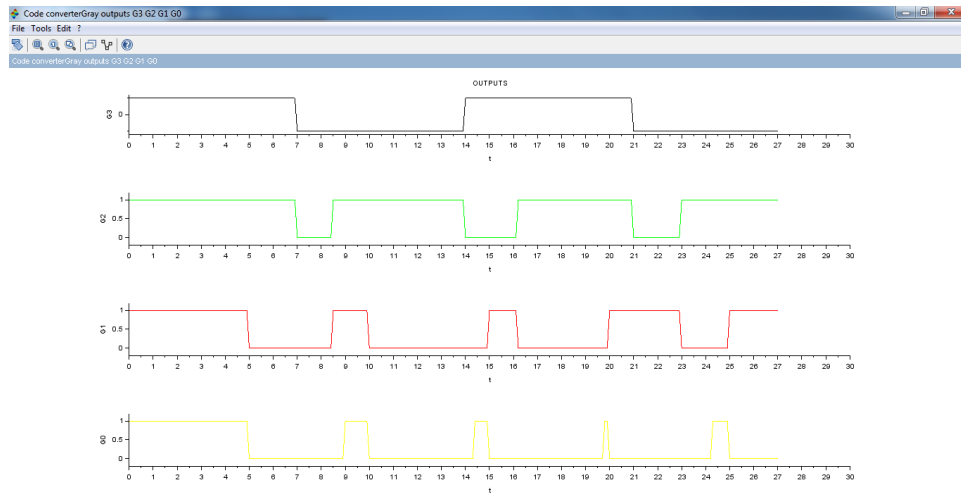


Figure 12.4: Binary to Gray code converter