Scilab Manual for Digital System Design Lab by Dr Ravindra Patil Electronics and Telecommunication Engineering M.H. Saboo Siddik College of Engineering[1]

Solutions provided by
Dr Ravindra Patil
Electronics and Telecommunication Engineering
University Of Mumbai

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[1]Funded by a grant from the National Mission on Education through ICT, http://spoken-tutorial.org/NMEICT-Intro. This Scilab Manual and Scilab codes written in it can be downloaded from the "Migrated Labs" section at the website http://scilab.in

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Experiment: 1

Design and simulate basic gates: NOT ,AND,OR,NOR,NAND,EXOR

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This code can be downloaded from the website wwww.scilab.in

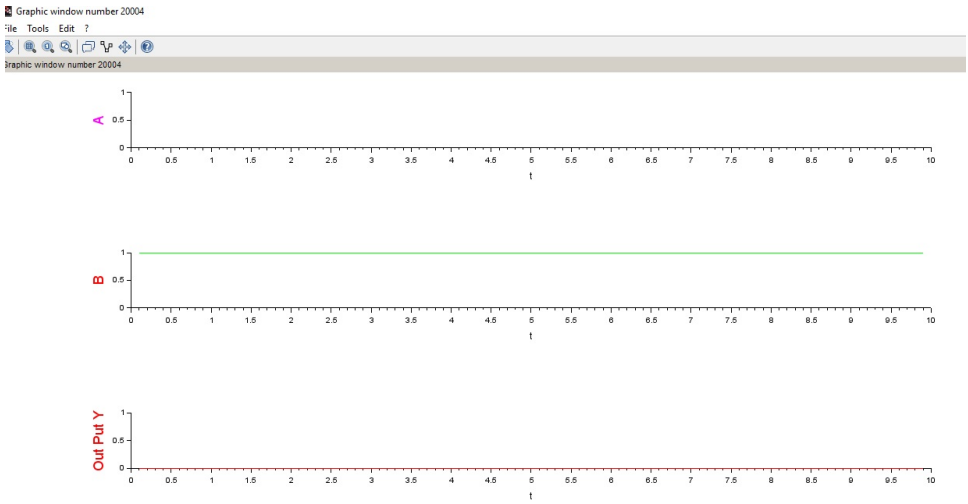

Figure 1.1: AND GATE

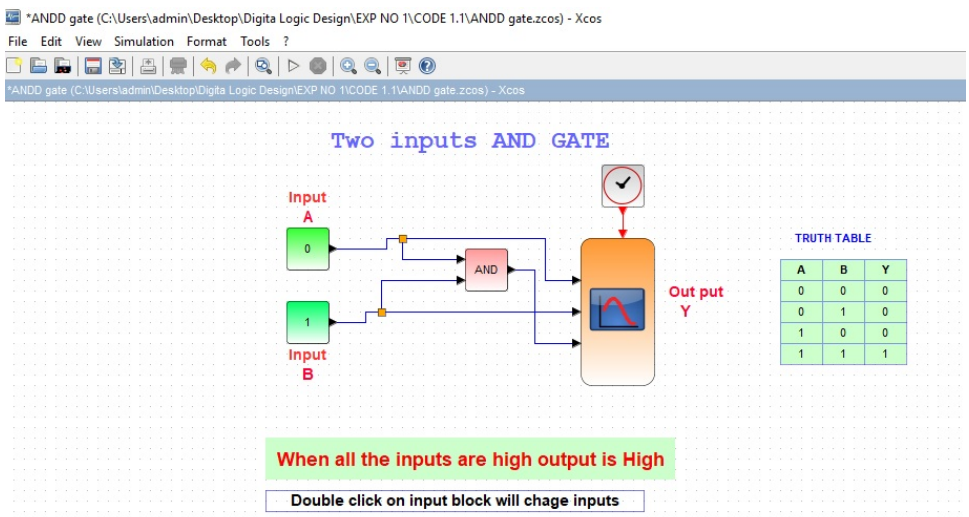

Figure 1.2: AND GATE

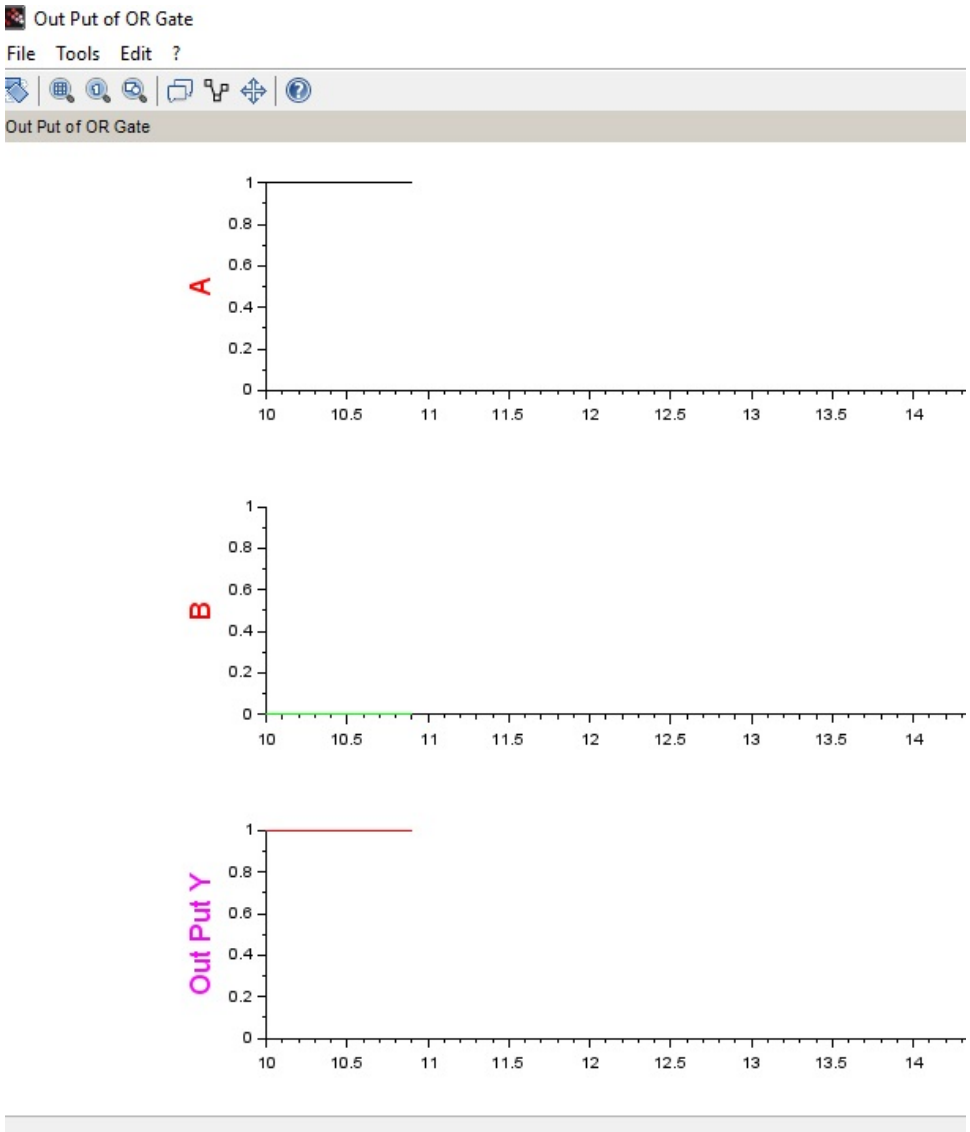

Figure 1.3: OR GATE

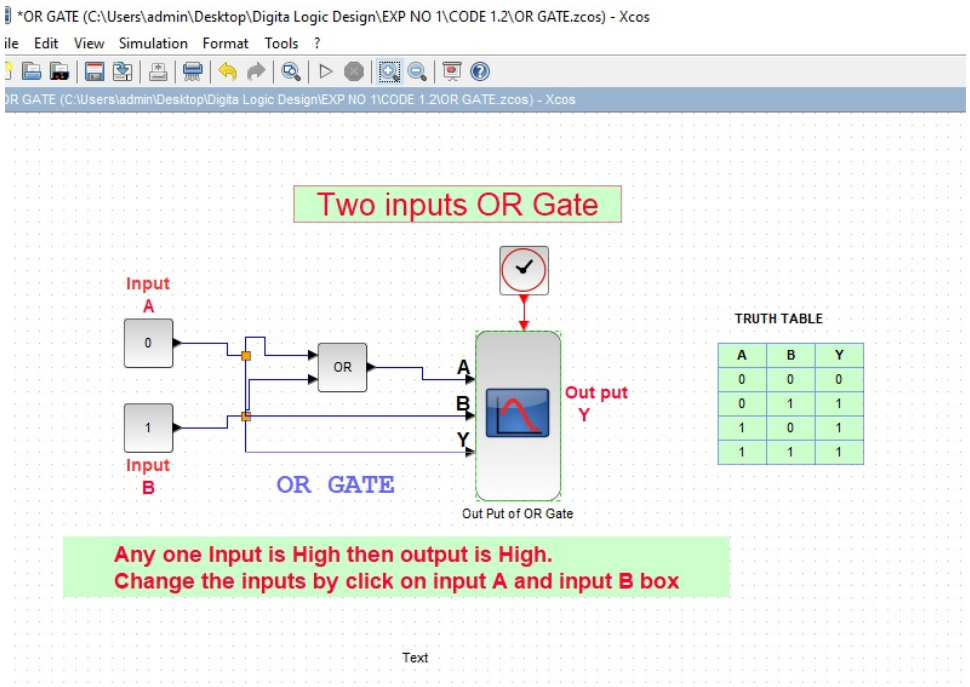

Figure 1.4: OR GATE

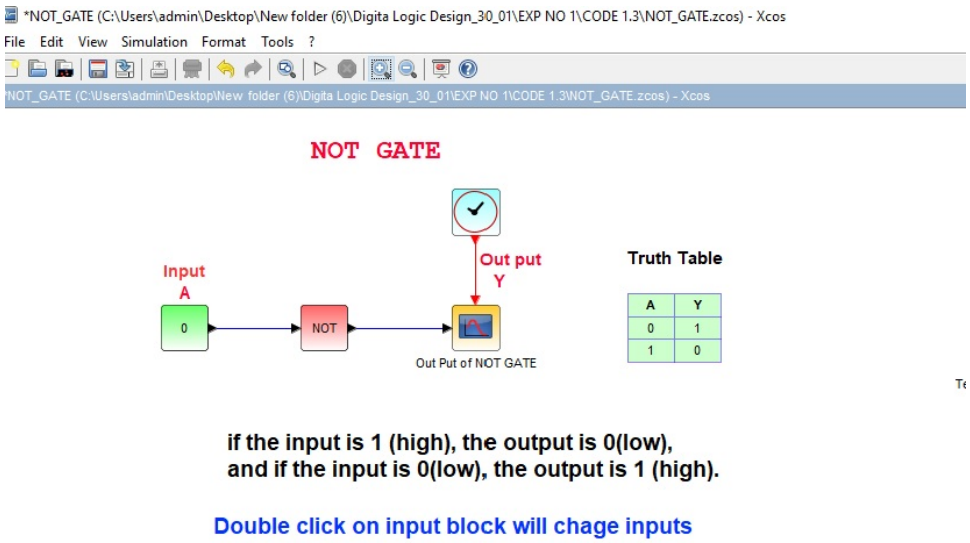

Figure 1.5: NOT GATE

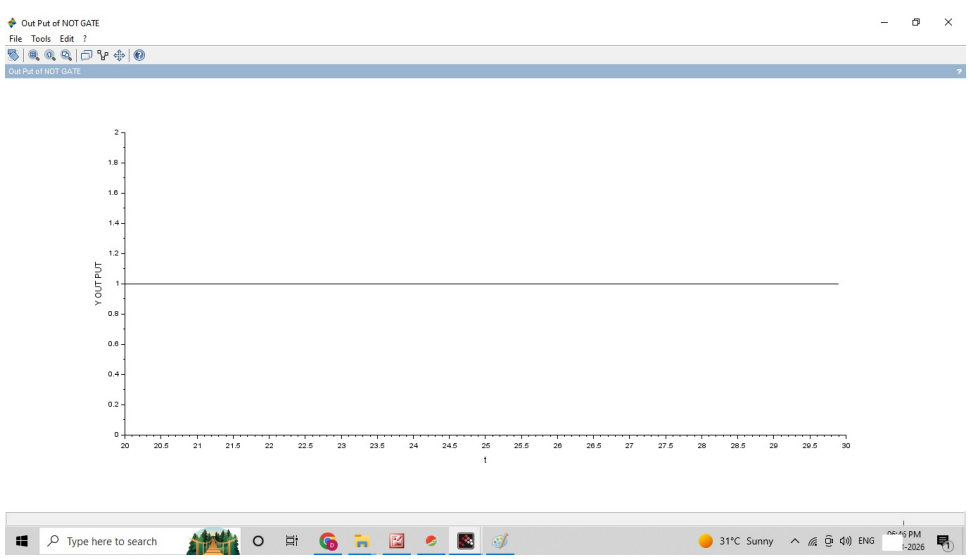

Figure 1.6: NOT GATE

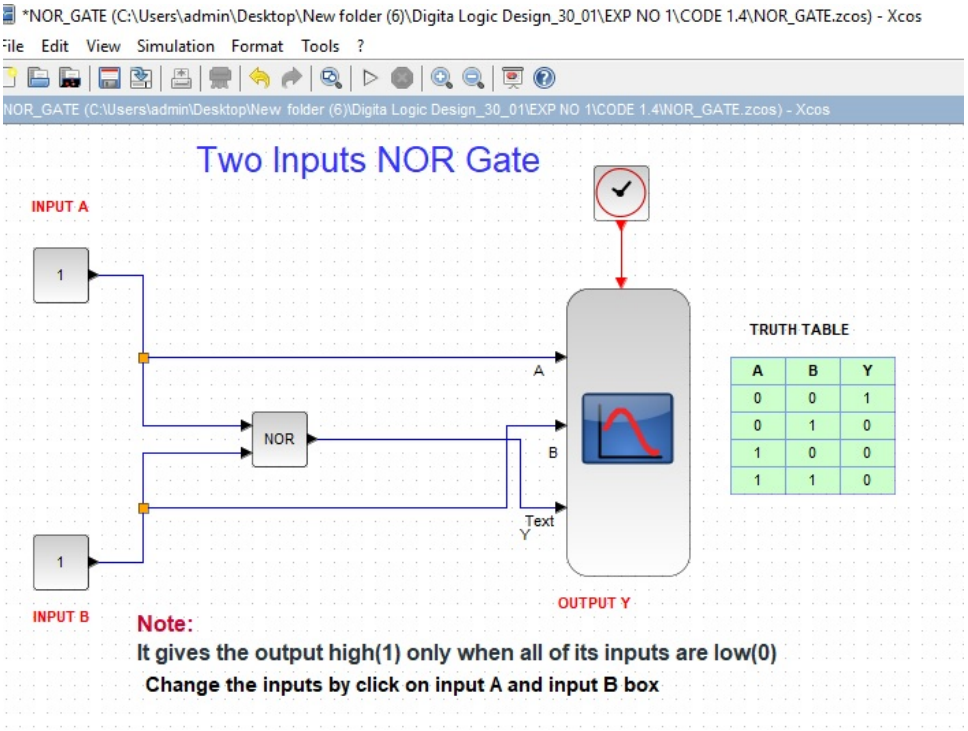

Figure 1.7: NOR GATE

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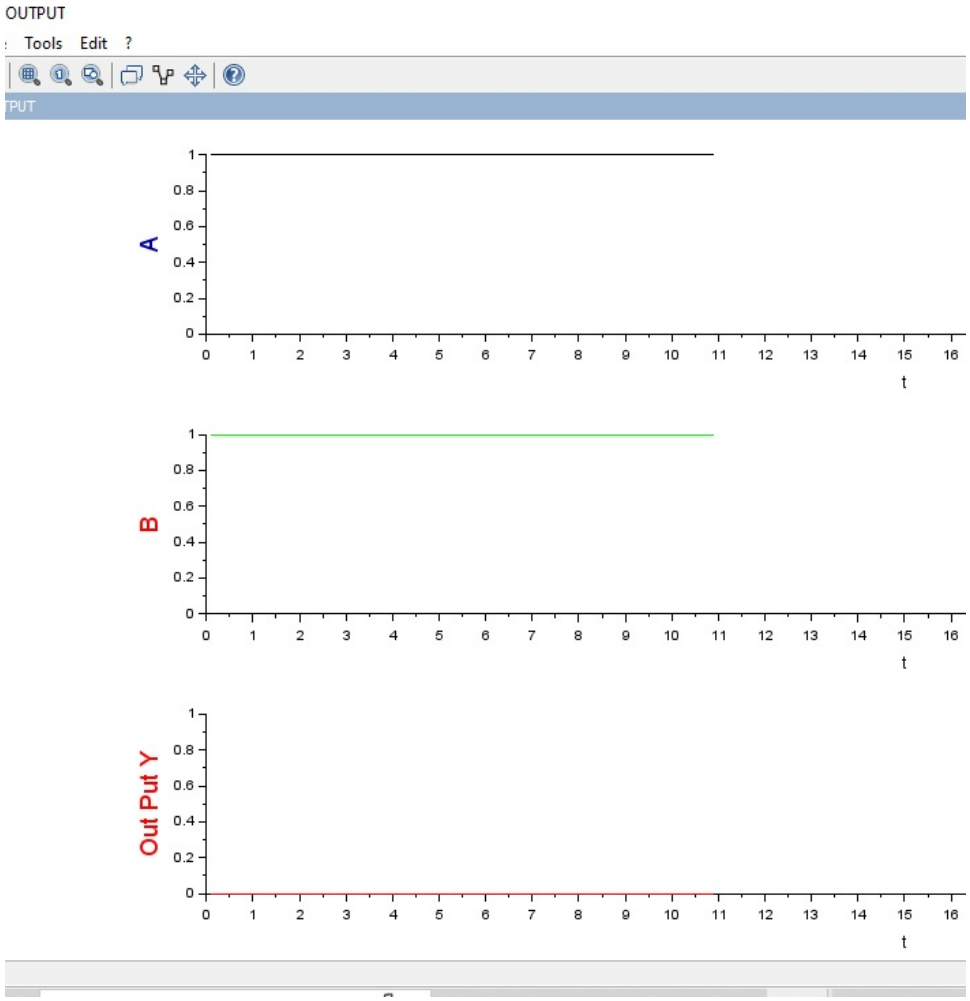

Figure 1.8: NOR GATE

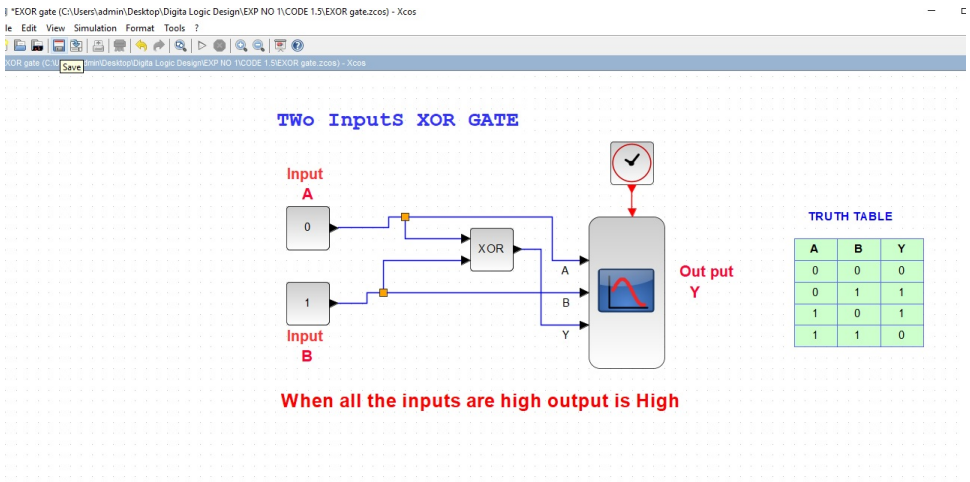

Figure 1.9: XOR GATE

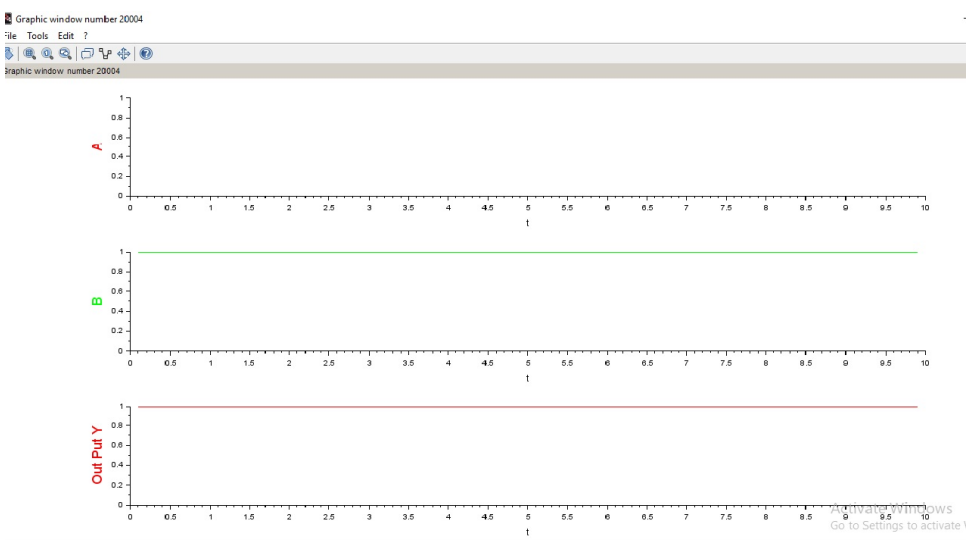

Figure 1.10: XOR GATE

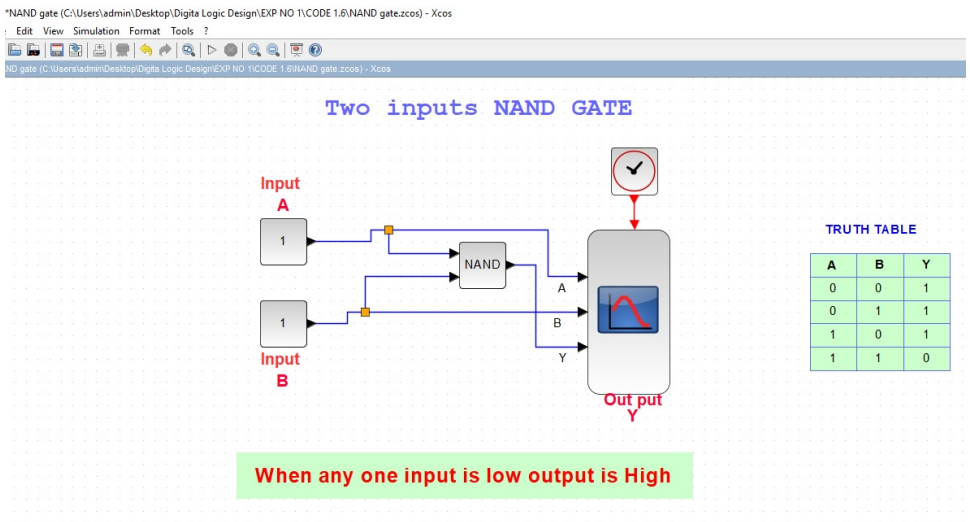

Figure 1.11: NAND GATE

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Figure 1.12: NAND GATE

Experiment: 2

Design and simulate AND, OR, NOT, EXOR gates using Universal gates: NAND and NOR.

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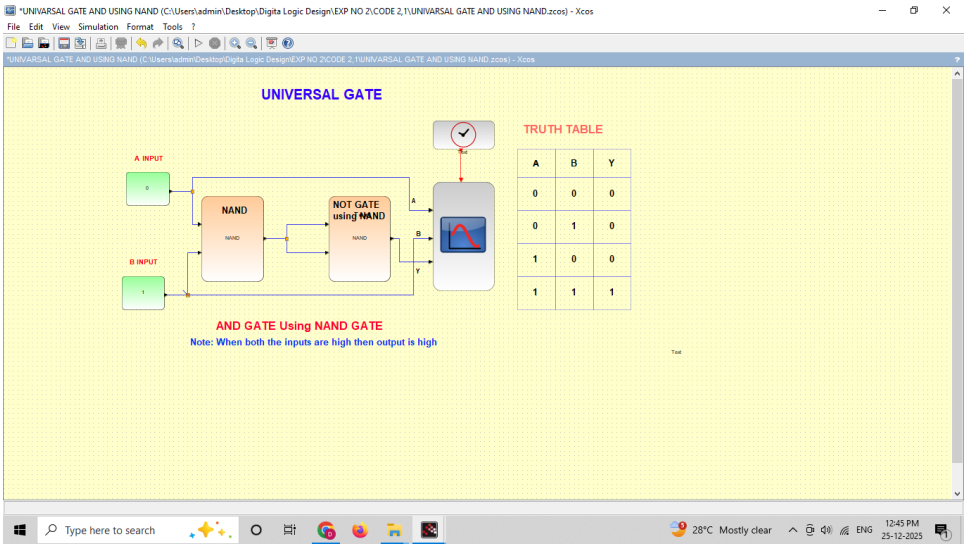

Figure 2.1: AND GATE USING NAND

Figure 2.2: AND GATE USING NAND

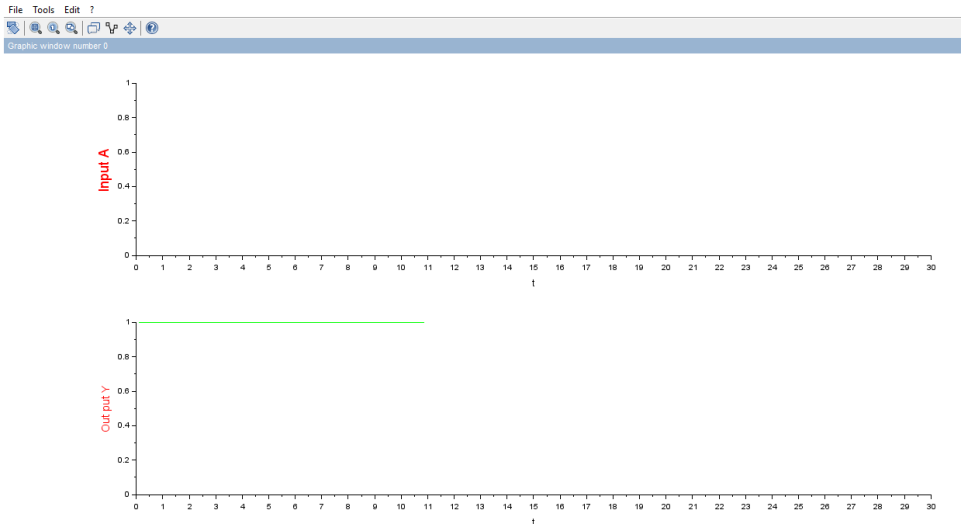

Figure 2.3: NOT GATE USING NAND GATE

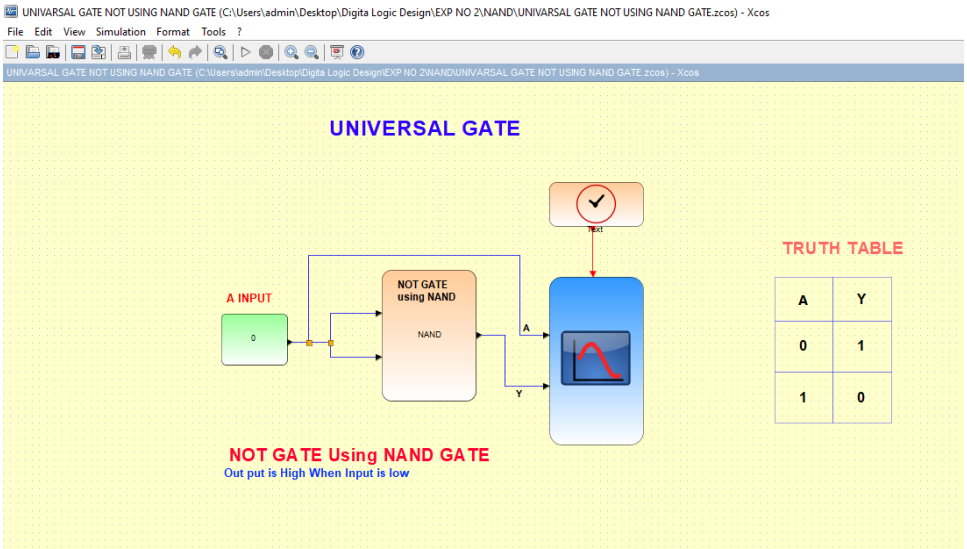

Figure 2.4: NOT GATE USING NAND GATE

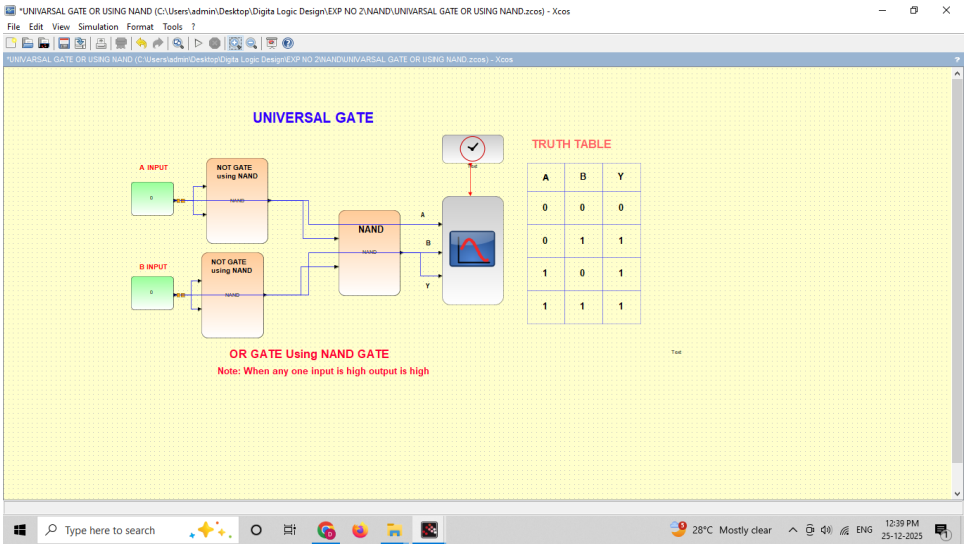

Figure 2.5: OR GATE USING NAND GATE

Figure 2.6: OR GATE USING NAND GATE

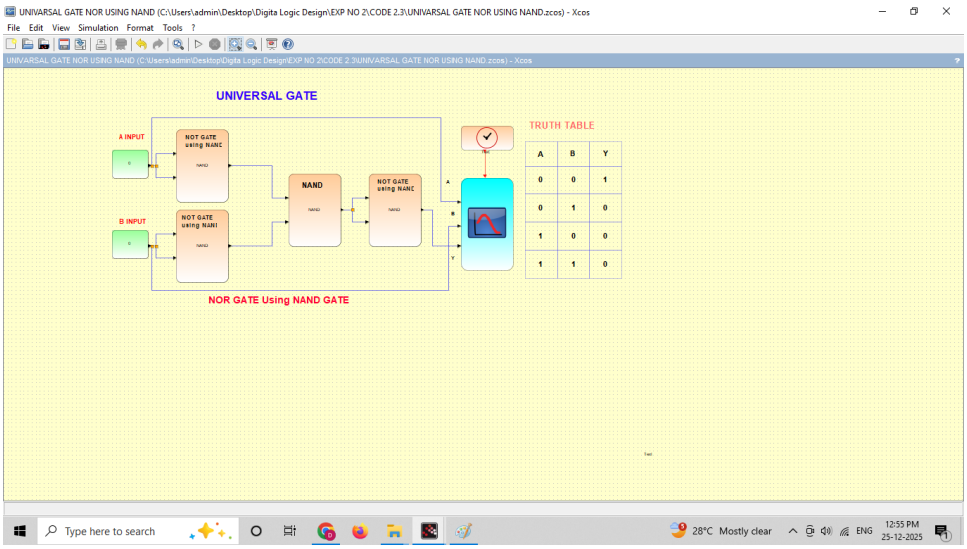

Figure 2.7: NOR GATE USING NAND GATE

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This code can be downloaded from the website wwww.scilab.in

This code can be downloaded from the website wwww.scilab.in

Figure 2.8: NOR GATE USING NAND GATE

Figure 2.9: XOR GATE USING NAND GATE

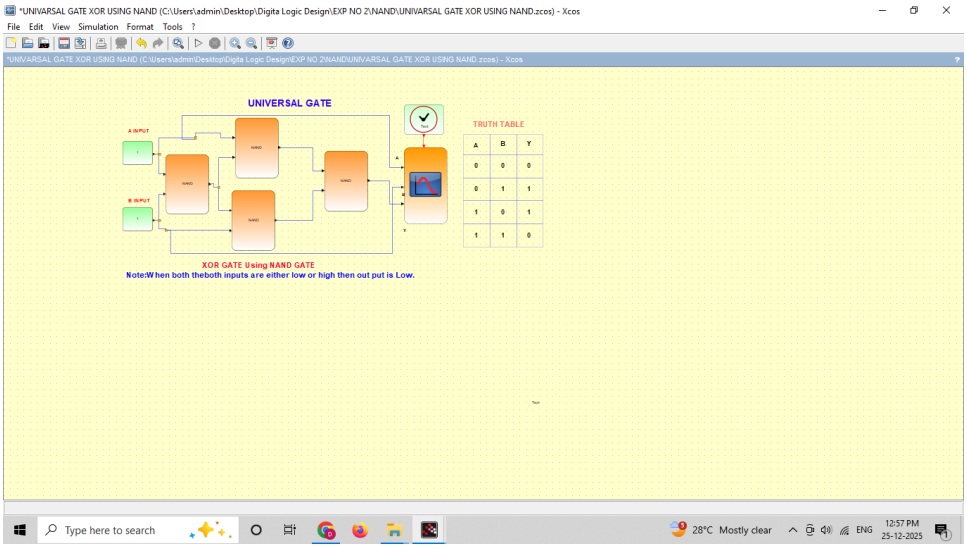

Figure 2.10: XOR GATE USING NAND GATE

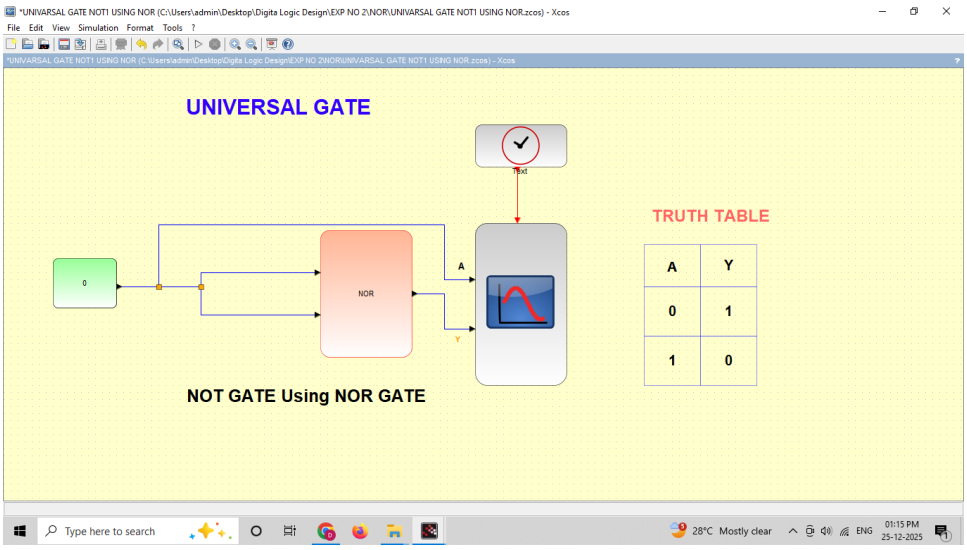

Figure 2.11: NOT GATE USING NAND GATE

Figure 2.12: NOT GATE USING NAND GATE

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This code can be downloaded from the website wwww.scilab.in

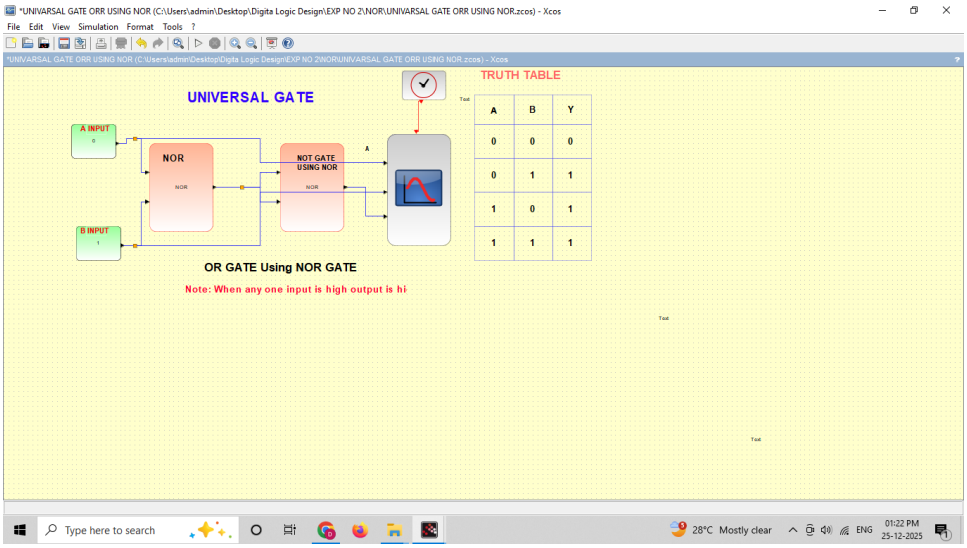

Figure 2.13: OR GATE USING NOR GATE

Figure 2.14: OR GATE USING NOR GATE

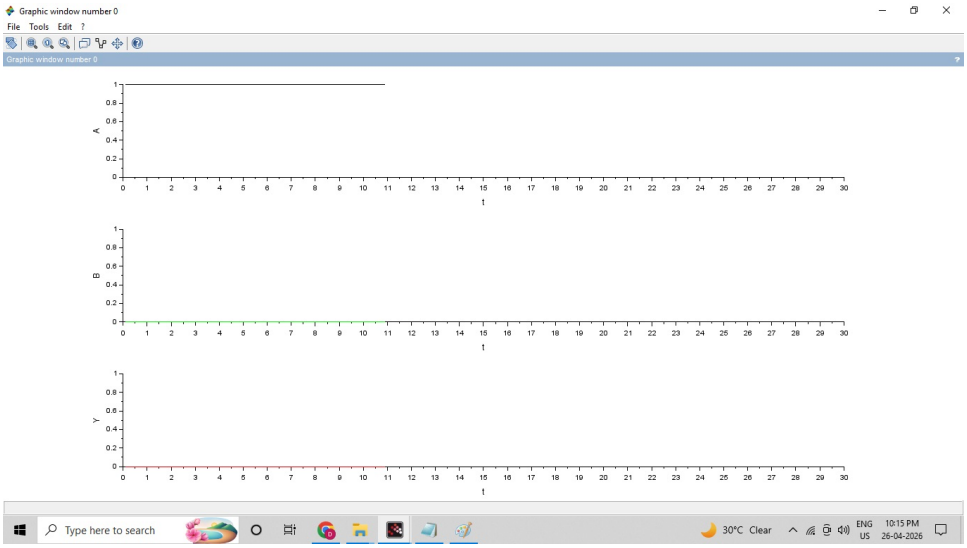

Figure 2.15: AND GATE USING NORGATE

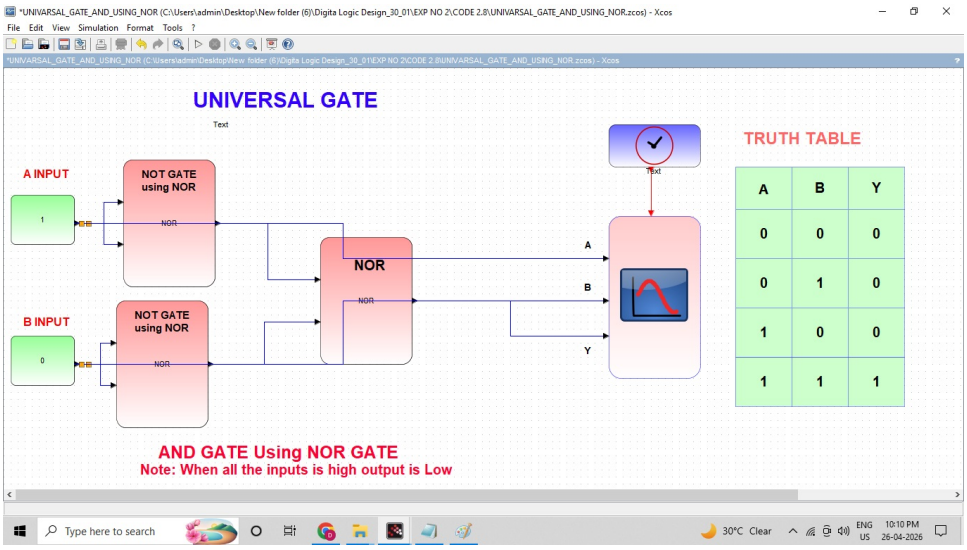

Figure 2.16: AND GATE USING NORGATE

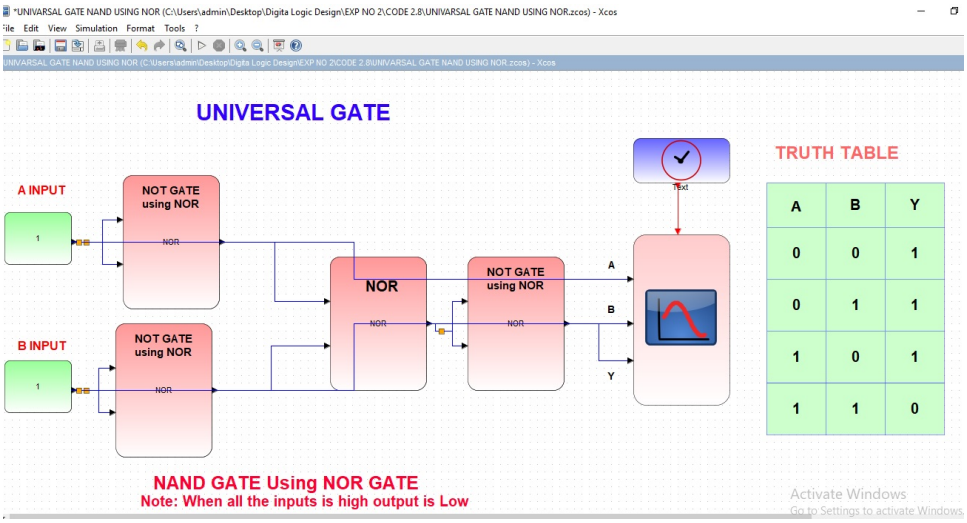

Figure 2.17: NAND GATE USING NOR GATE

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This code can be downloaded from the website wwww.scilab.in

This code can be downloaded from the website wwww.scilab.in

Figure 2.18: NAND GATE USING NOR GATE

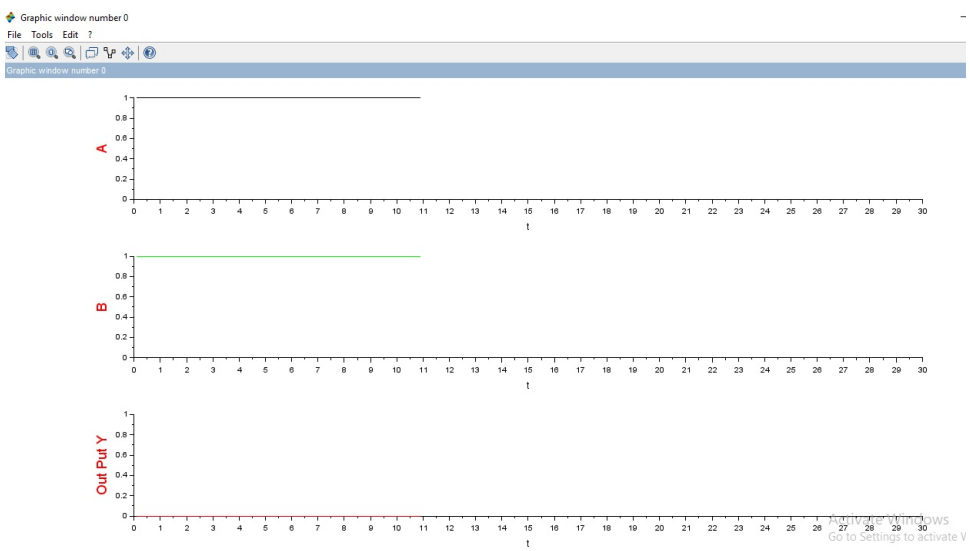

Figure 2.19: XOR GATE USING NOR GATE

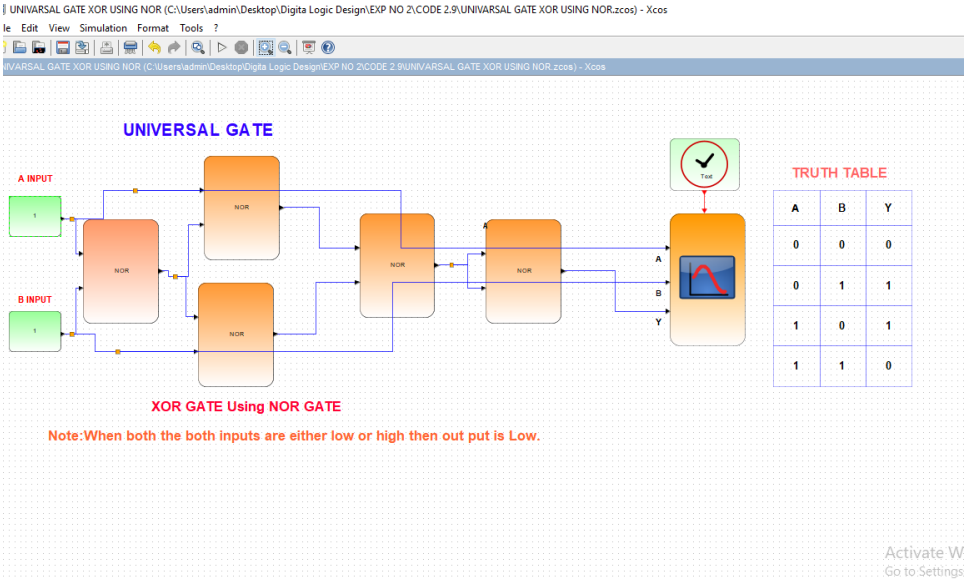

Figure 2.20: XOR GATE USING NOR GATE

Experiment: 3

Design and simulate digital circuits to perform Binary to Gray and Gray to Binary operations.

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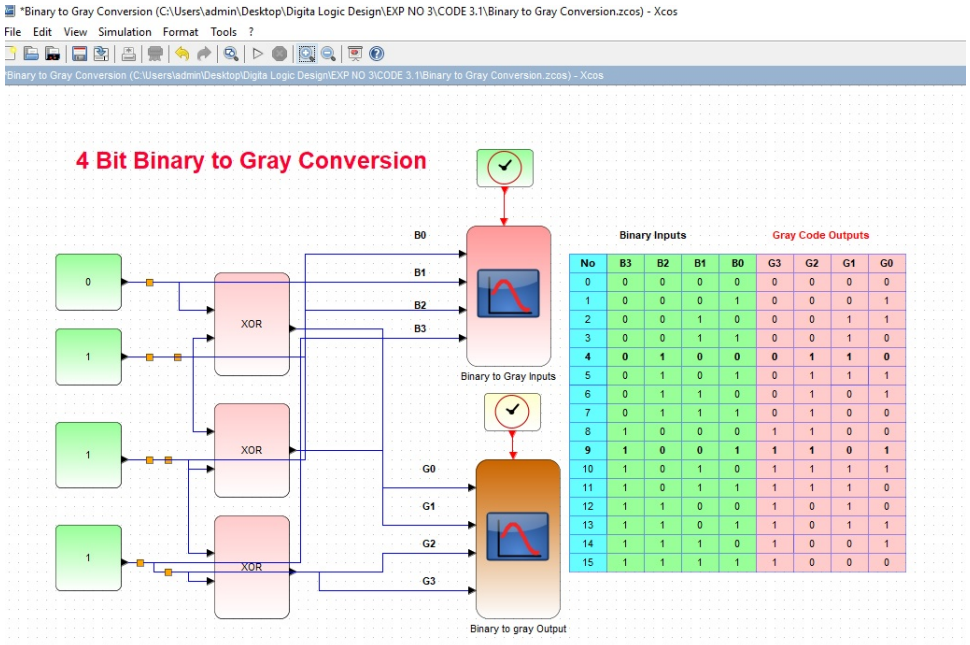


No	B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	**0**	**1**	**0**	**0**	**0**	**1**	**1**	**0**
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**1**
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

Figure 3.1: Binary to Gray code Converter

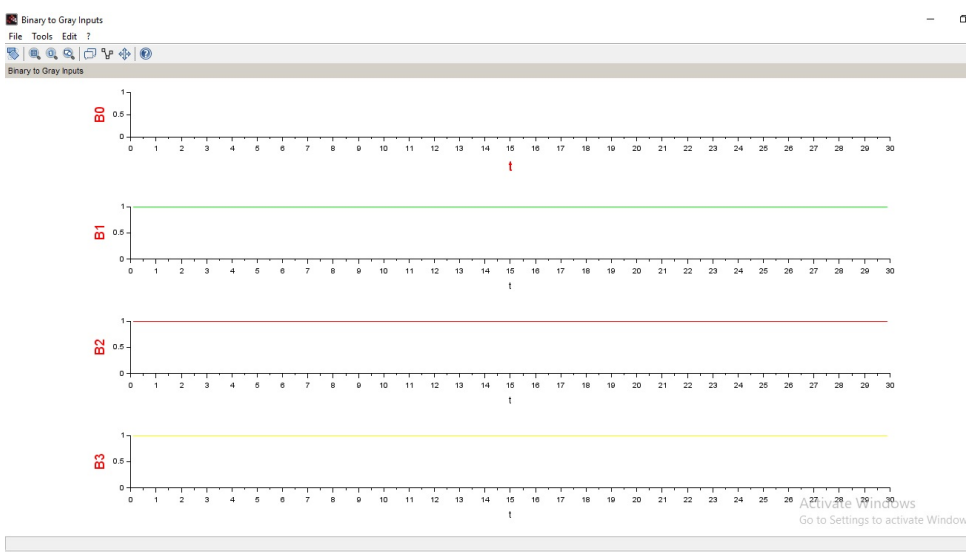


Figure 3.2: Binary to Gray code Converter

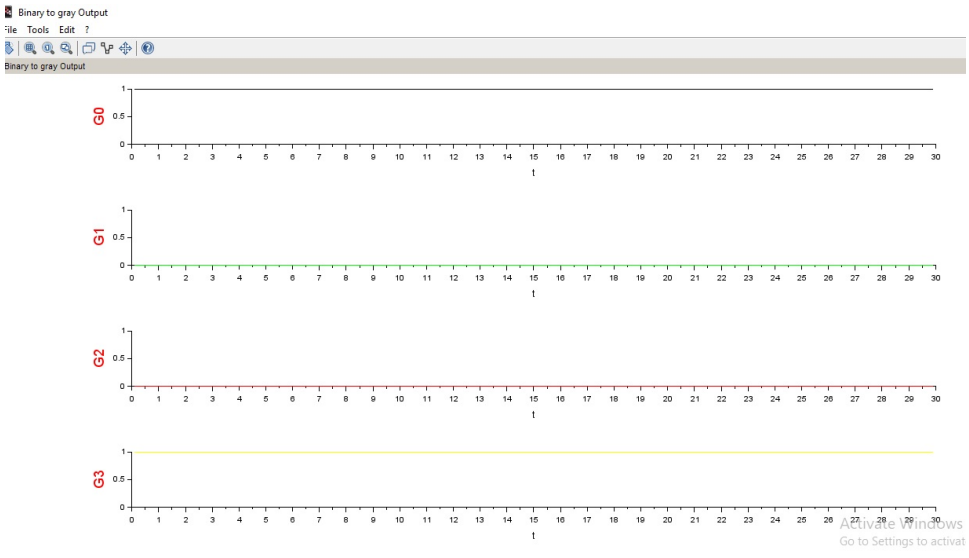
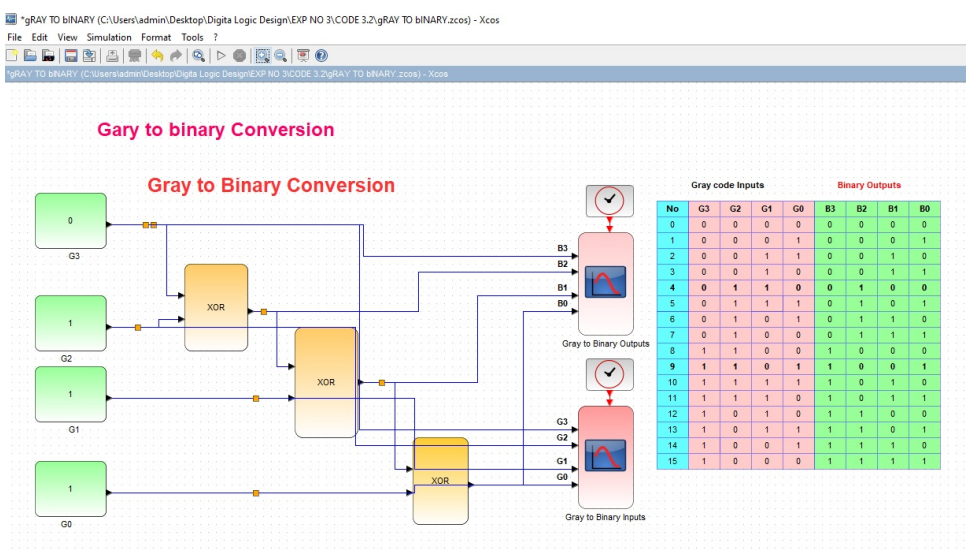


Figure 3.3: Binary to Gray code Converter



Gray code Inputs | Binary Outputs

No	G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**
5	0	1	1	1	0	1	0	1
6	0	1	0	1	0	1	1	0
7	0	1	0	0	0	1	1	1
8	1	1	0	0	1	0	0	0
9	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**1**
10	1	1	1	1	1	0	1	0
11	1	1	1	0	1	0	1	1
12	1	0	1	0	1	1	0	0
13	1	0	1	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	0	1	1	1	1

Figure 3.4: gray to binary code conversion

Figure 3.5: gray to binary code conversion

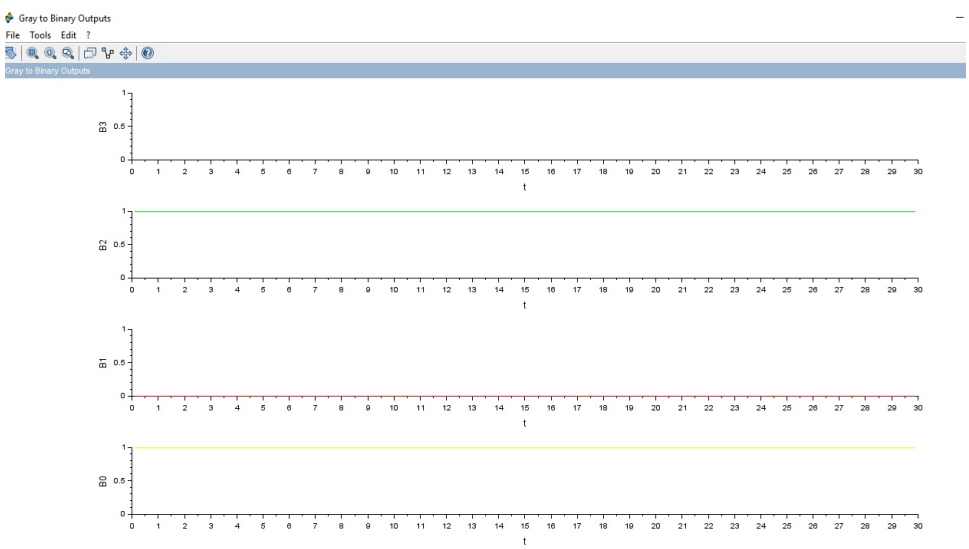


Figure 3.6: gray to binary code conversion

Experiment: 4

Design and simulate Magnitude Comparator.

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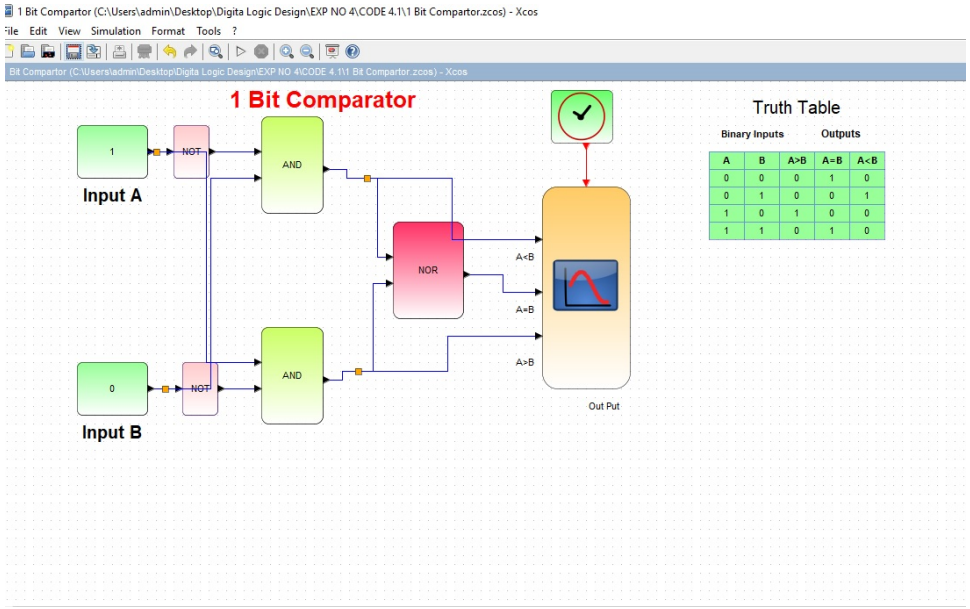

Figure 4.1: One bit Comparator

Figure 4.2: One bit Comparator

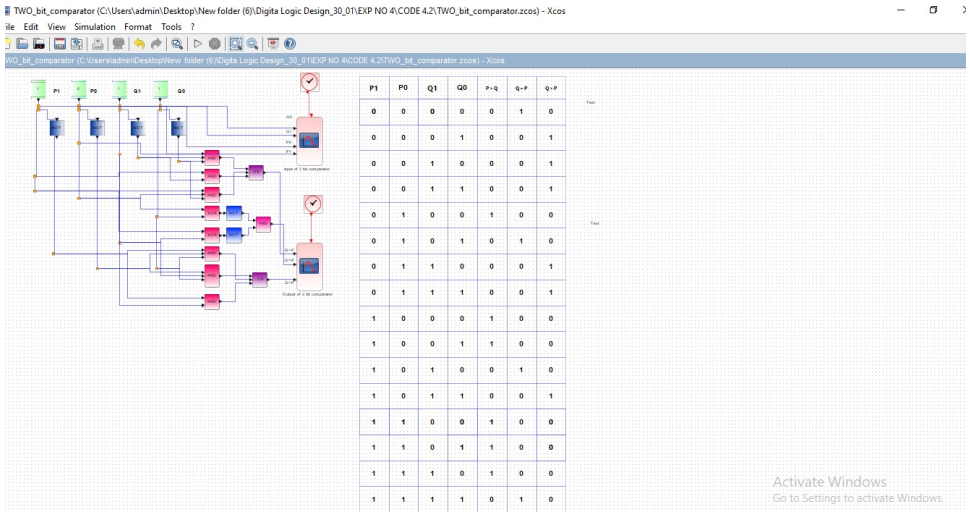

Figure 4.3: two bit comparator

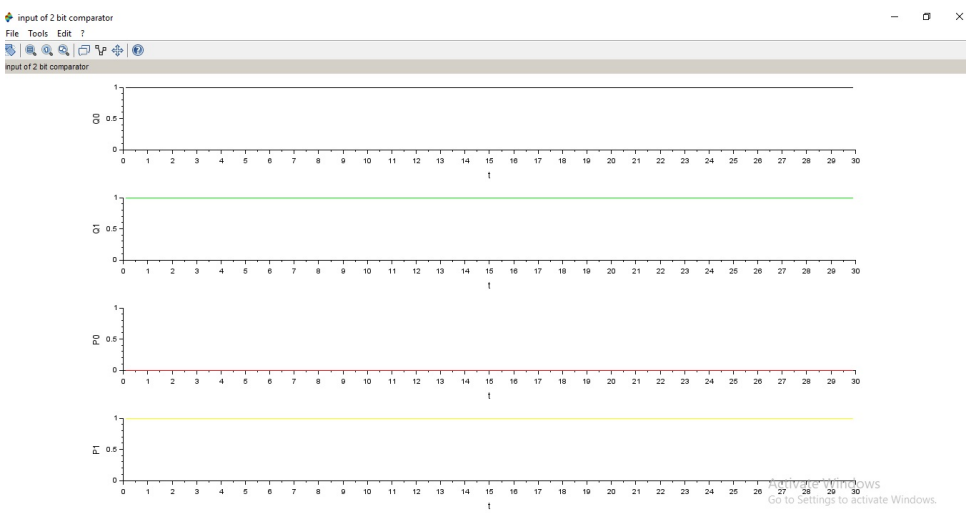

Figure 4.4: two bit comparator

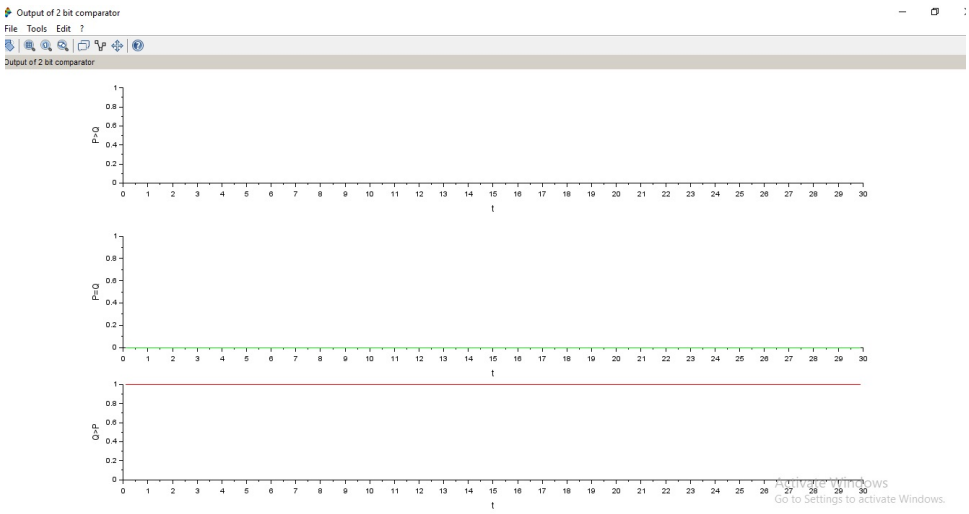

Figure 4.5: two bit comparator

Experiment: 5

Design and simulate parity generator and detector.

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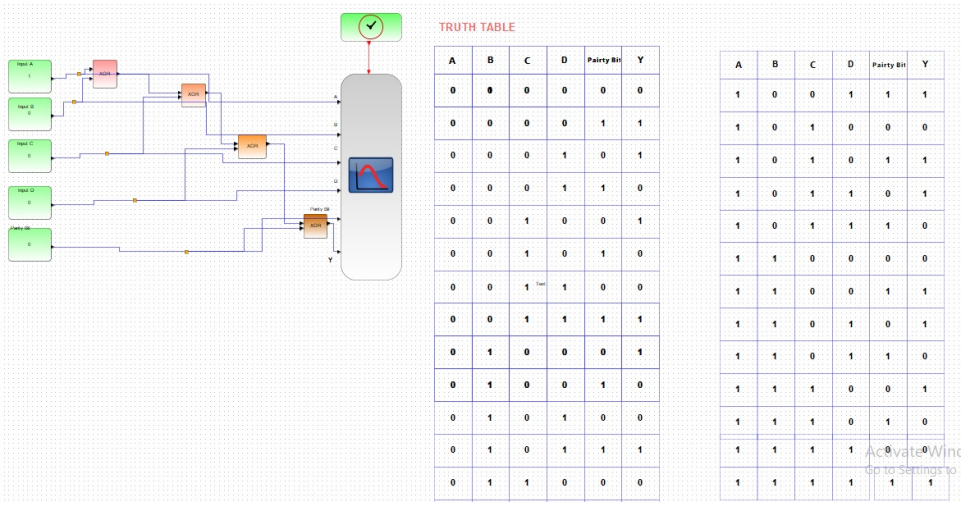


TRUTH TABLE

A	B	C	D	Pairty Bit	Y
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	1
0	1	1	0	0	0

A	B	C	D	Pairty Bit	Y
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	1

Figure 5.1: Parity Generator

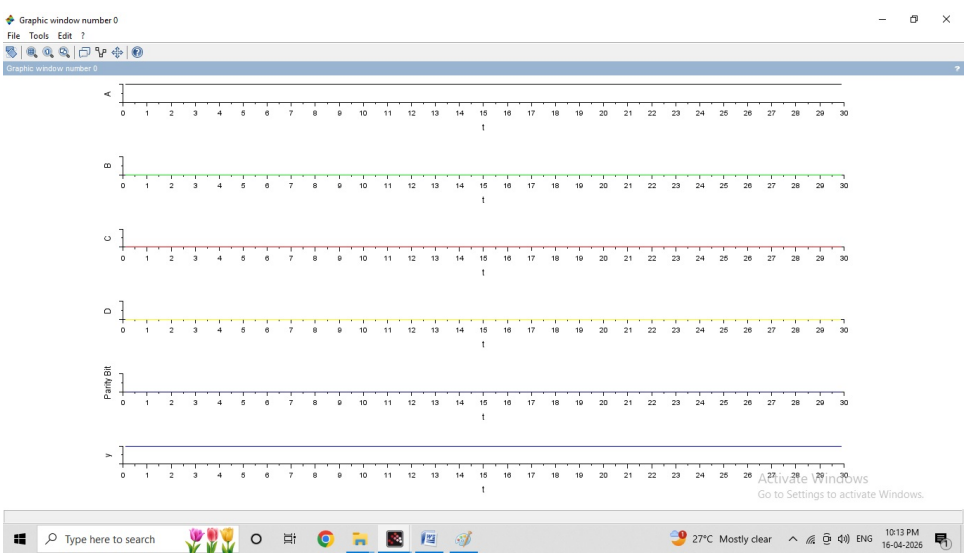


Figure 5.2: Parity Generator

Experiment: 6

Design and simulate Half adder, Full adder Circuits

This code can be downloaded from the website wwww.scilab.in

This code can be downloaded from the website wwww.scilab.in

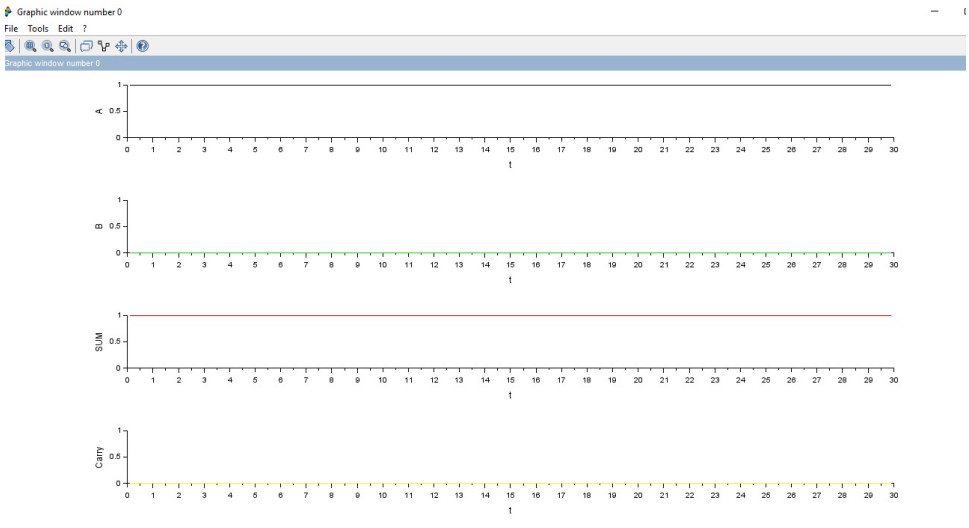


Figure 6.1: Half Adder

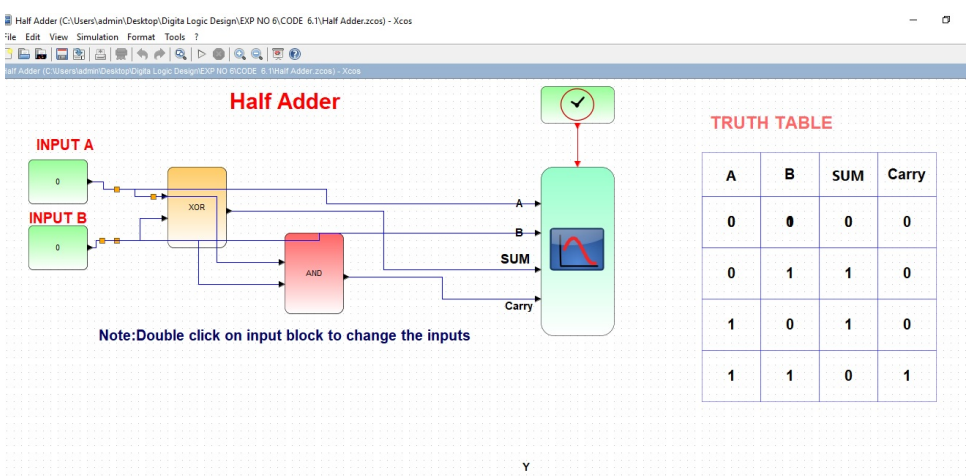
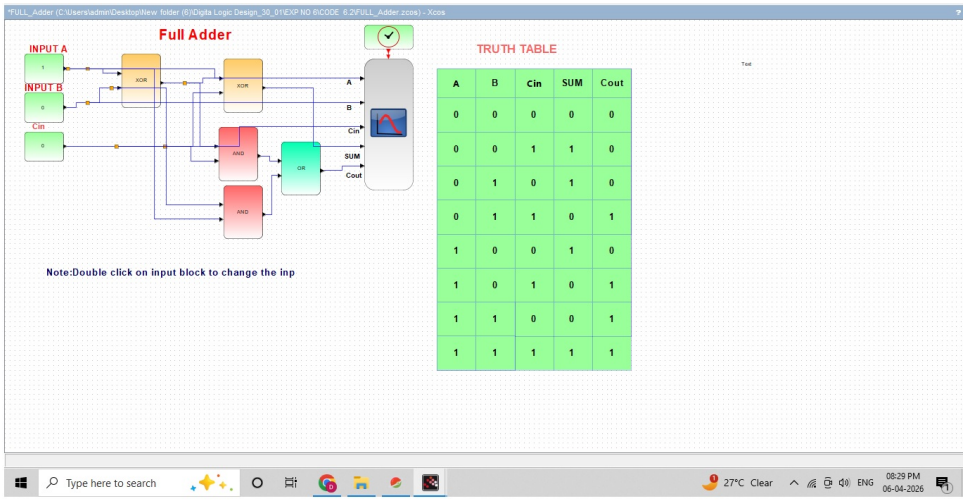


Figure 6.2: Half Adder



A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 6.3: Full Adder

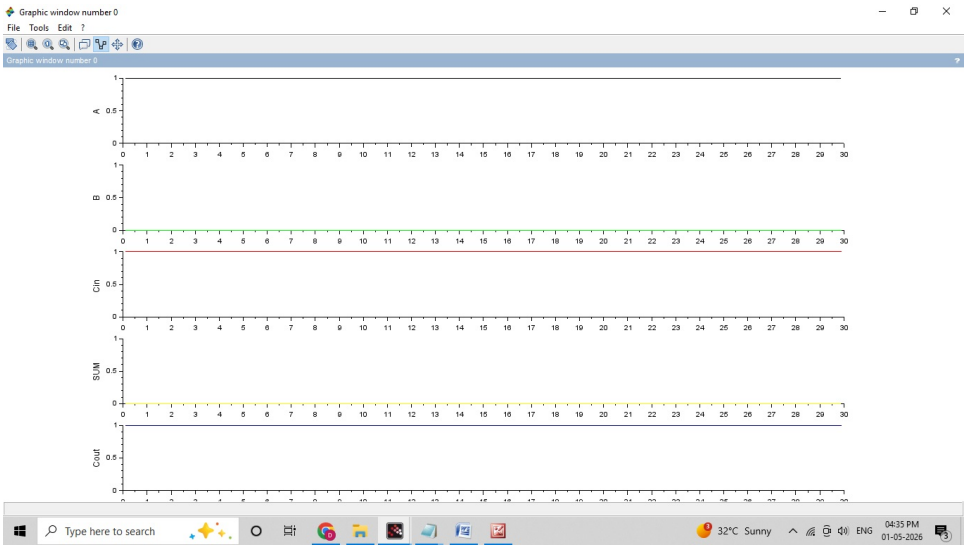


Figure 6.4: Full Adder

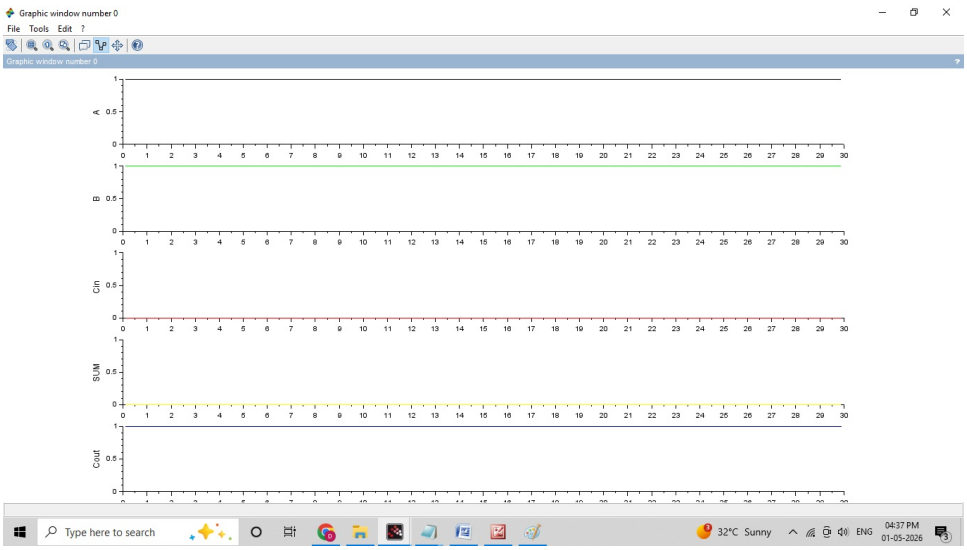


Figure 6.5: Full Adder

Experiment: 7

Design and simulate Half subtractor and Full subtractor circuits.

This code can be downloaded from the website wwww.scilab.in

This code can be downloaded from the website wwww.scilab.in

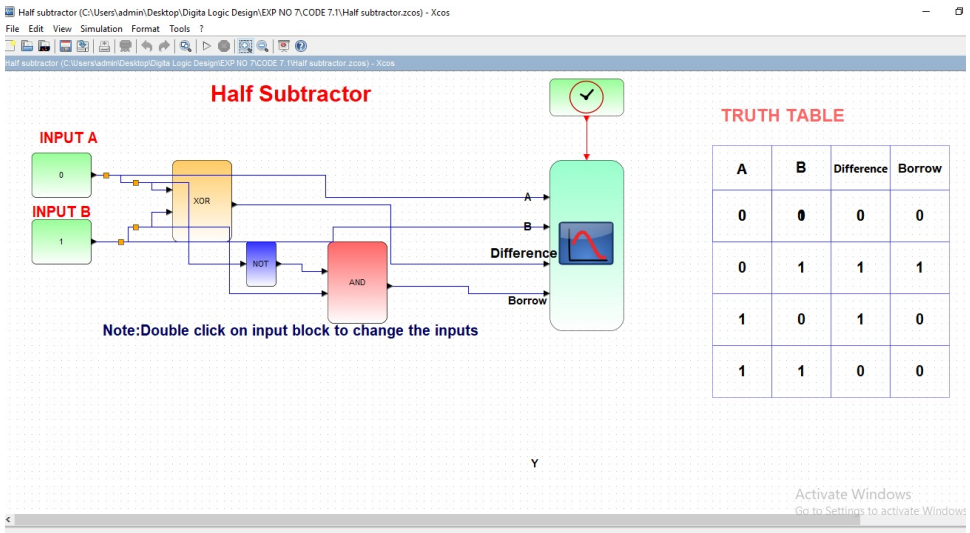


Figure 7.1: Half Subtractor

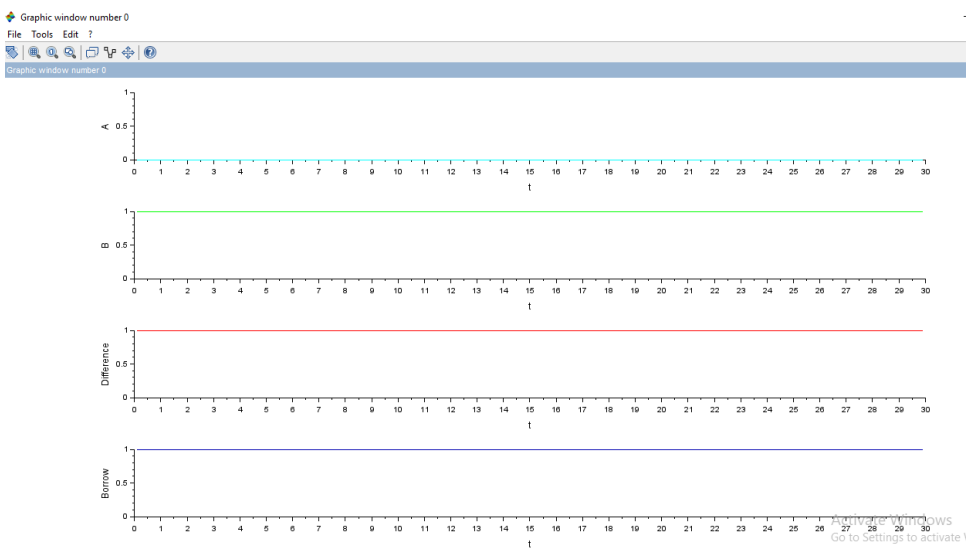


Figure 7.2: Half Subtractor

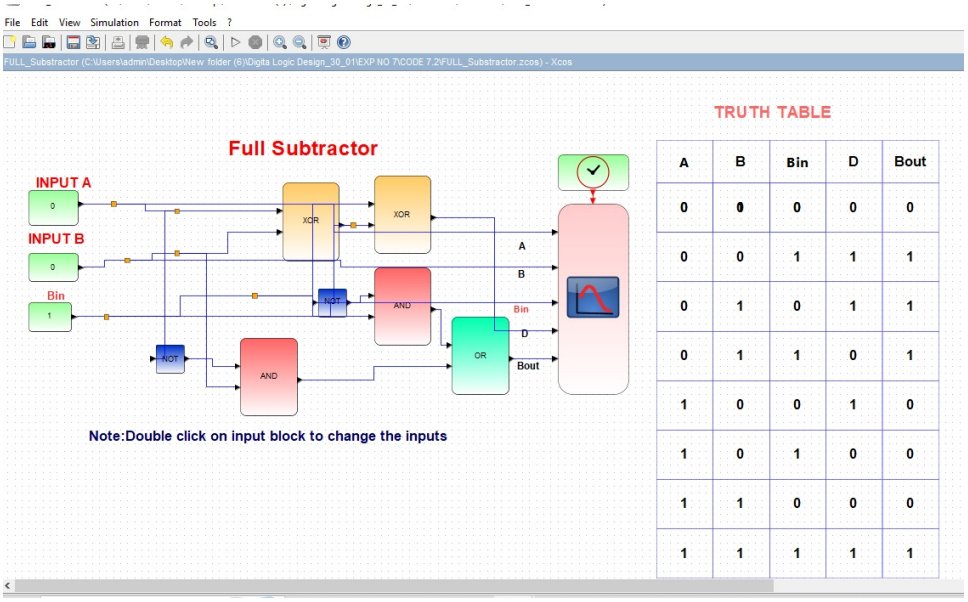


Figure 7.3: Full Subtractor

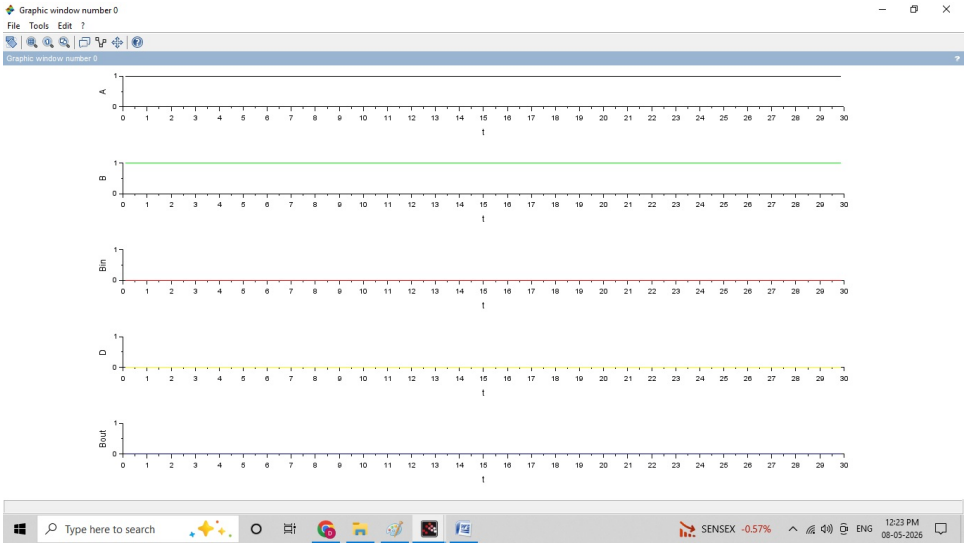


Figure 7.4: Full Subtractor

Experiment: 8

Design and simulate encoder and decoder circuits.

This code can be downloaded from the website wwww.scilab.in This code

can be downloaded from the website wwww.scilab.in

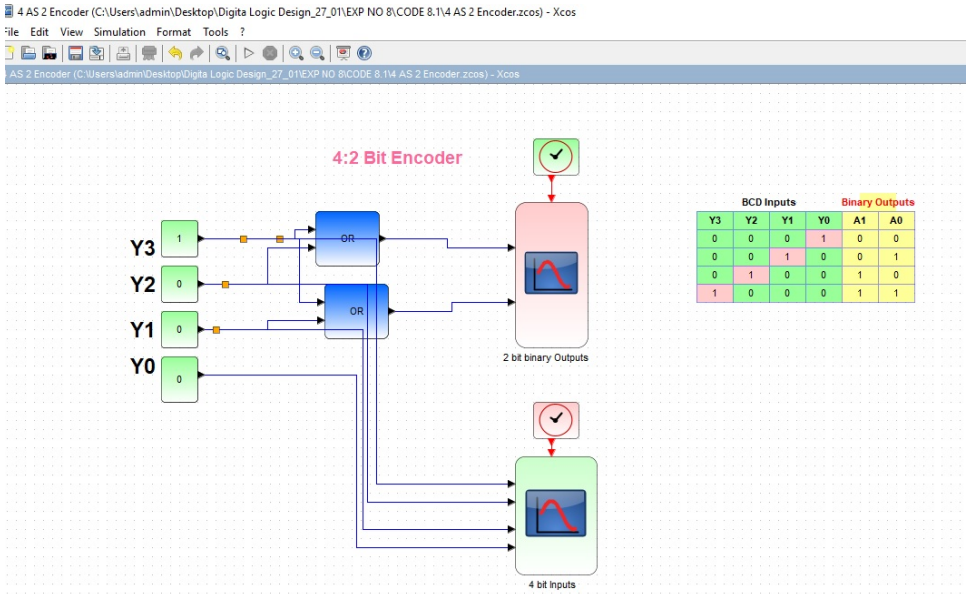


Figure 8.1: Four as Two bit encoder

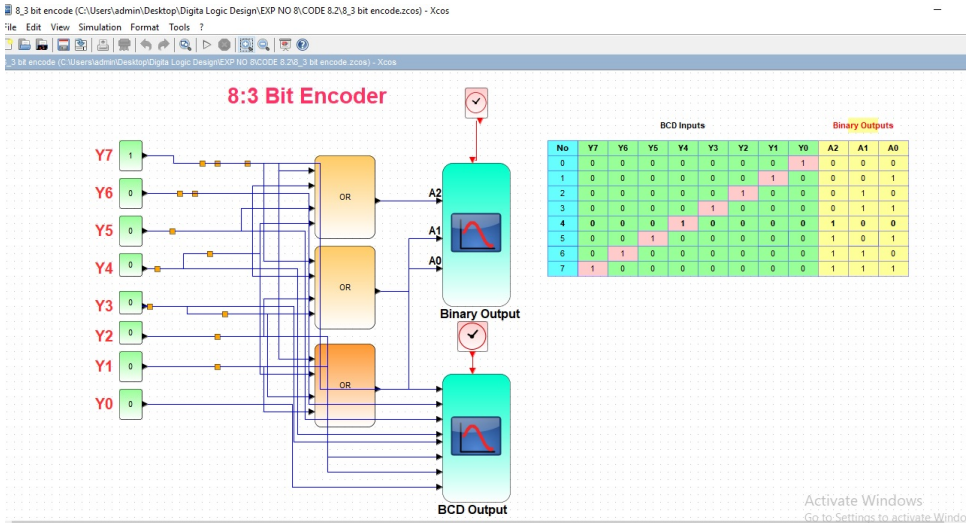


Figure 8.2: Eight AS TO THREE BIT ENCODER

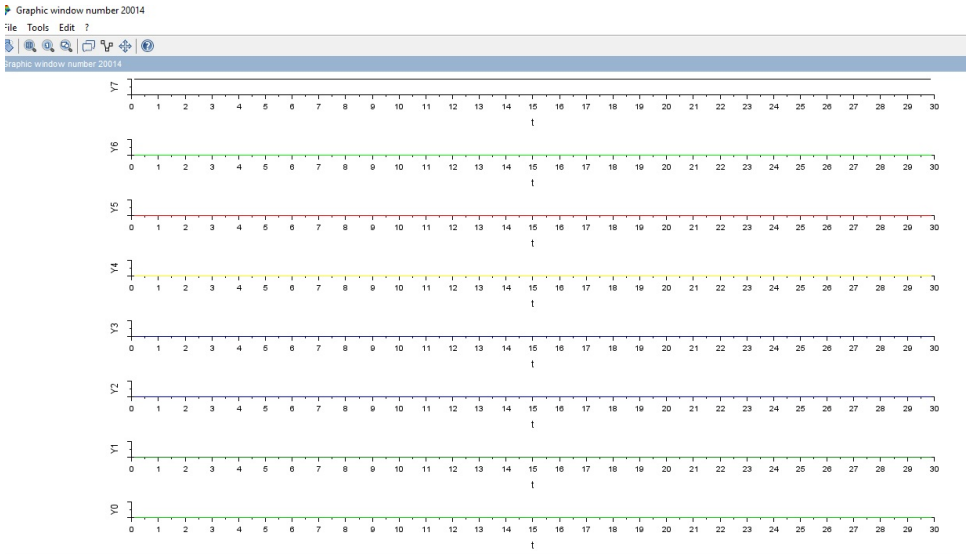


Figure 8.3: Eight AS TO THREE BIT ENCODER

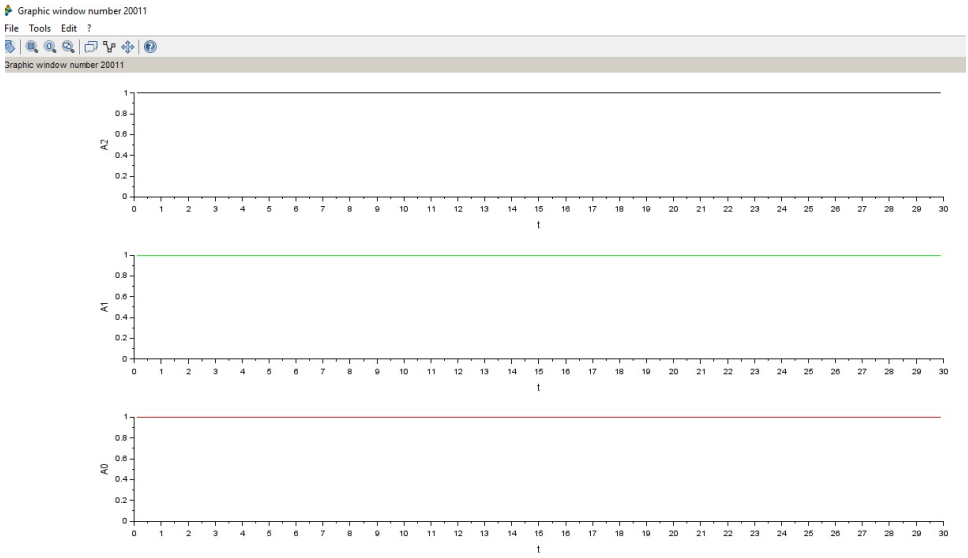


Figure 8.4: Eight AS TO THREE BIT ENCODER

Experiment: 9

Design and simulate decoder circuits.

This code can be downloaded from the website wwww.scilab.in

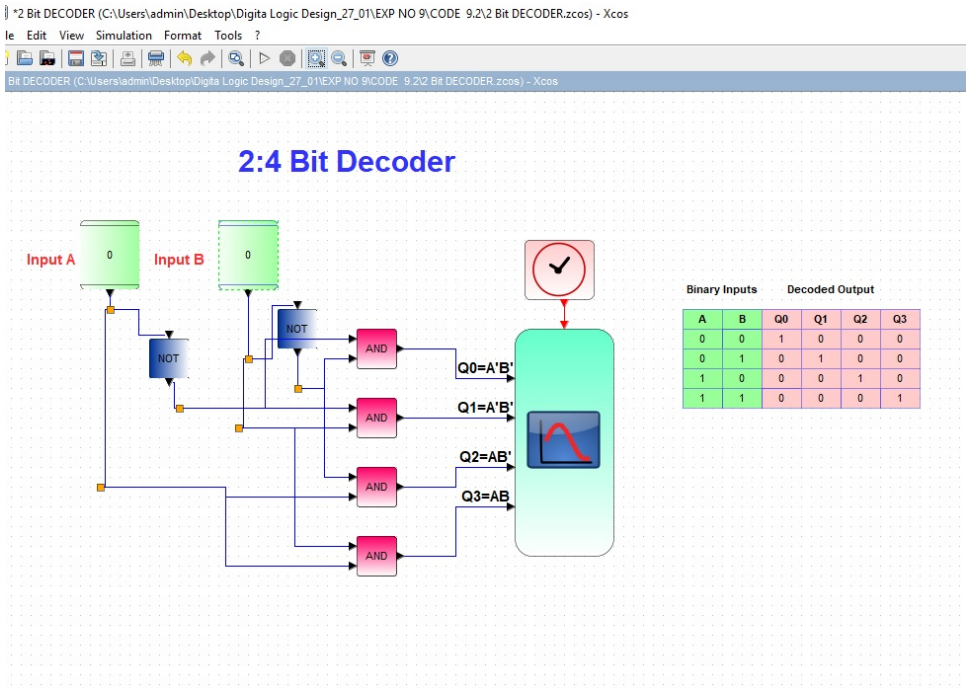


Figure 9.1: TWO BIT DECODER

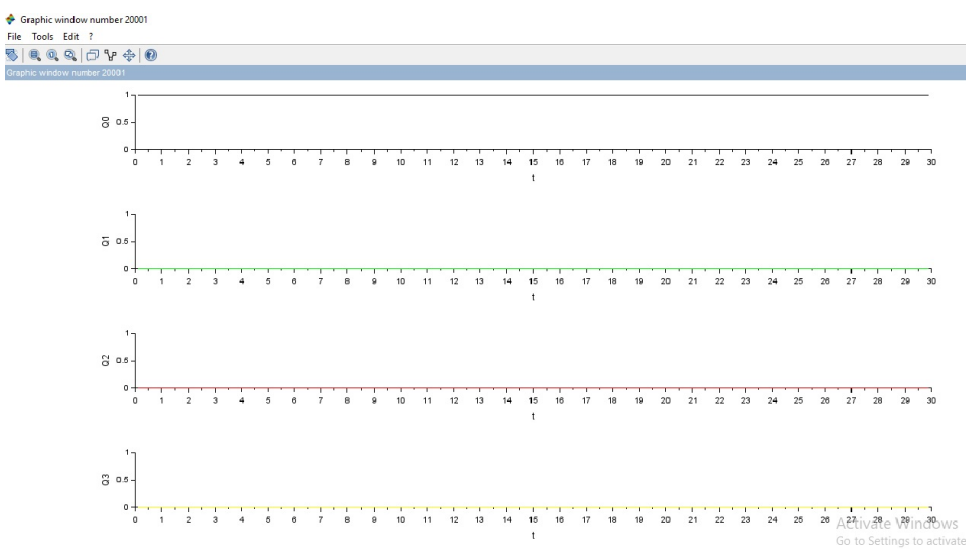


Figure 9.2: TWO BIT DECODER

Experiment: 10

Design and simulate 2:1,4:1 Multiplexer.

This code can be downloaded from the website wwww.scilab.in

This code can be downloaded from the website wwww.scilab.in

Figure 10.1: TWO AS TO ONE MULTIPLEXER

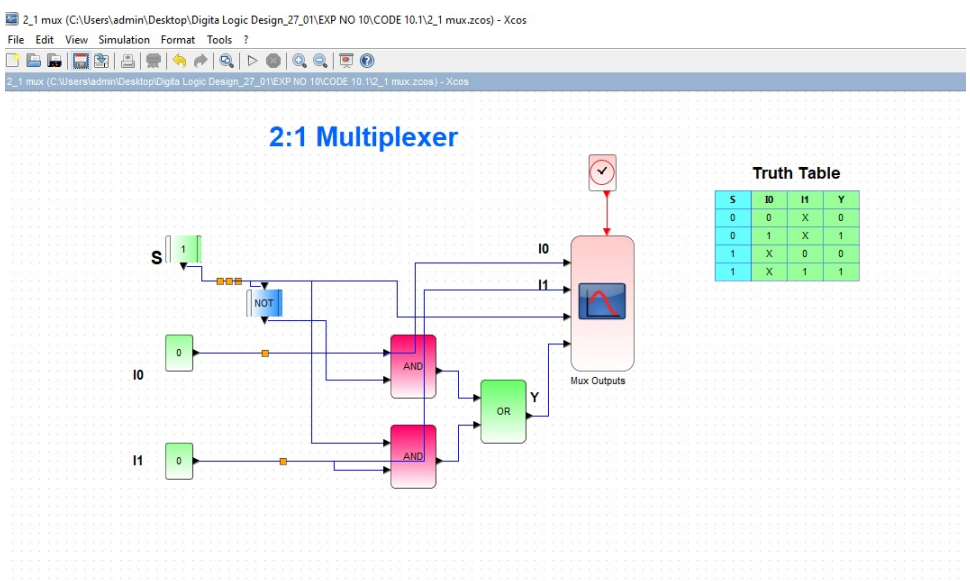


Figure 10.2: TWO AS TO ONE MULTIPLEXER

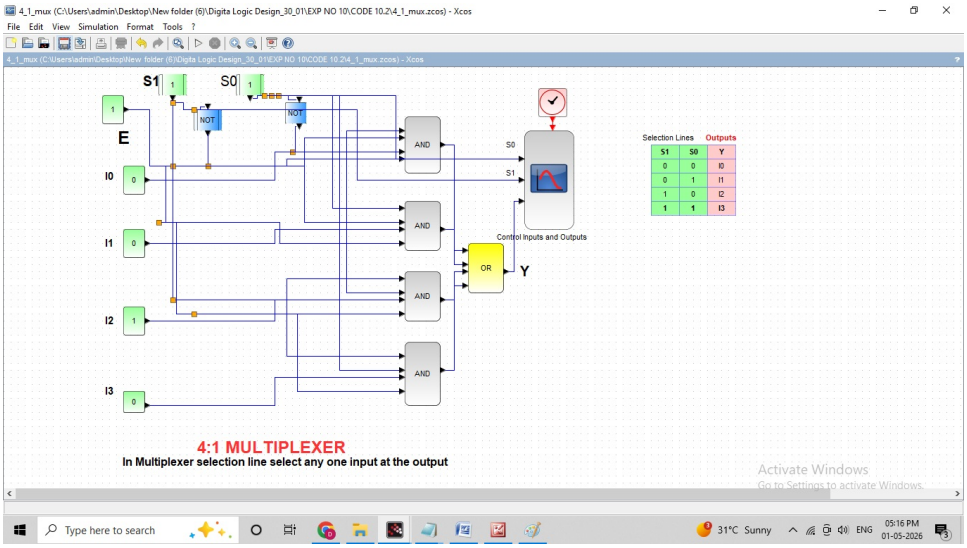


Figure 10.3: Four as to one Multiplexer

Figure 10.4: Four as to one Multiplexer

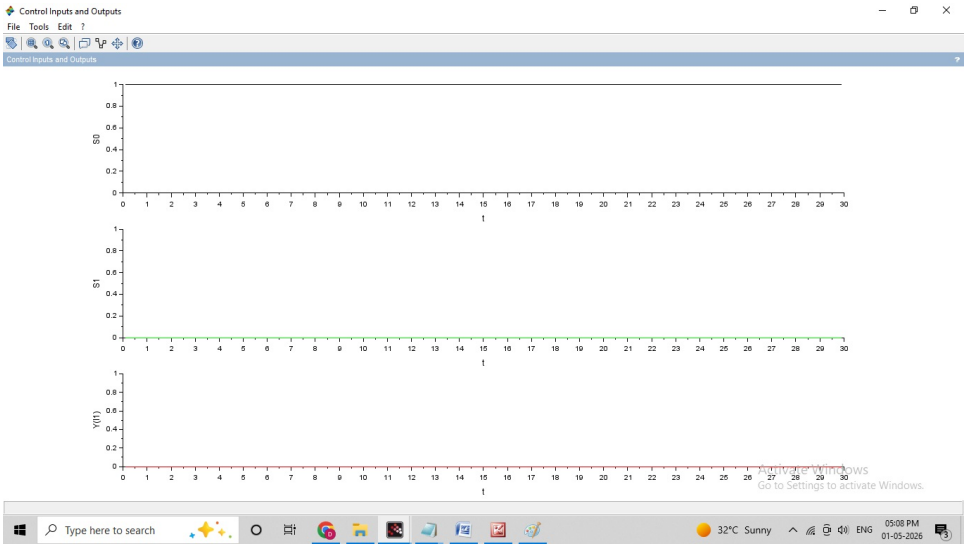


Figure 10.5: Four as to one Multiplexer

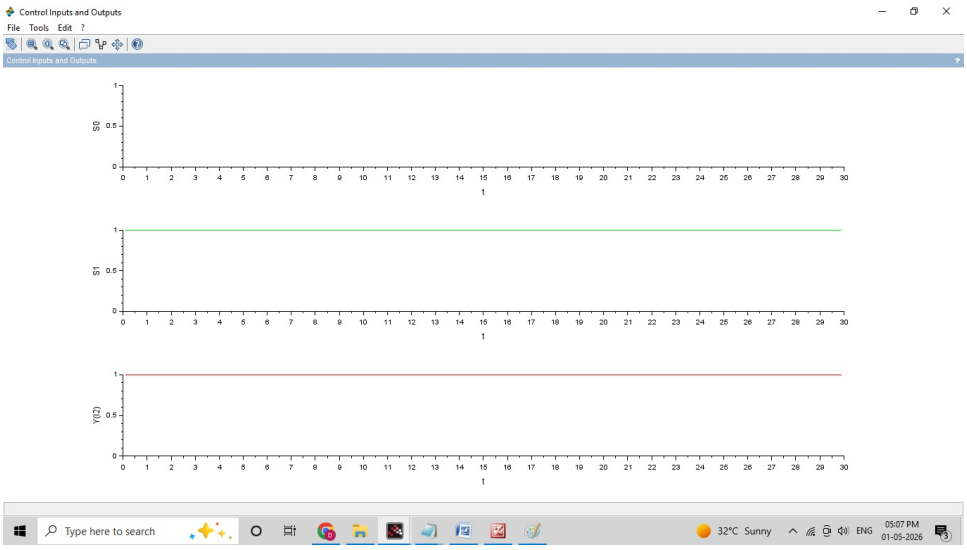


Figure 10.6: Four as to one Multiplexer

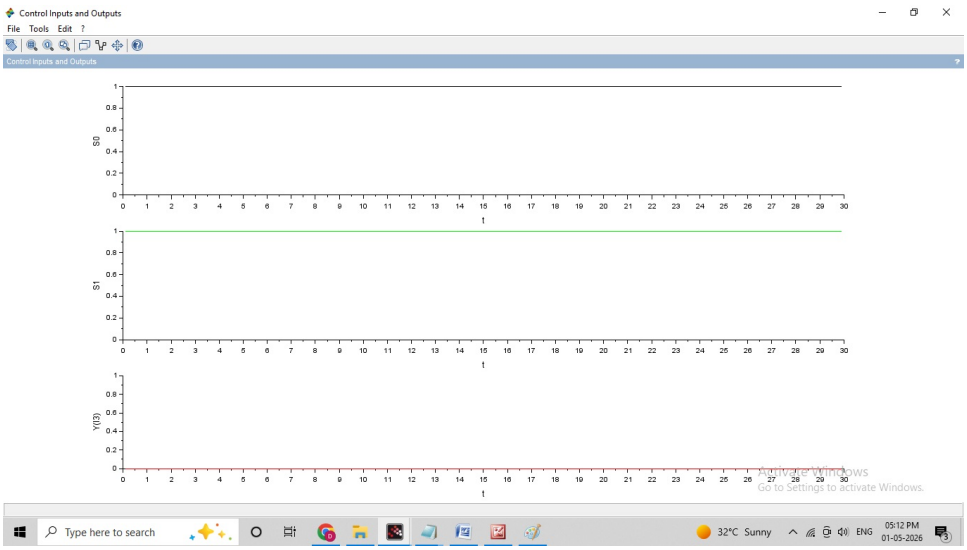


Figure 10.7: Four as to one Multiplexer

Experiment: 11

Design and simulate 1:2. 1:4De Multiplexer.

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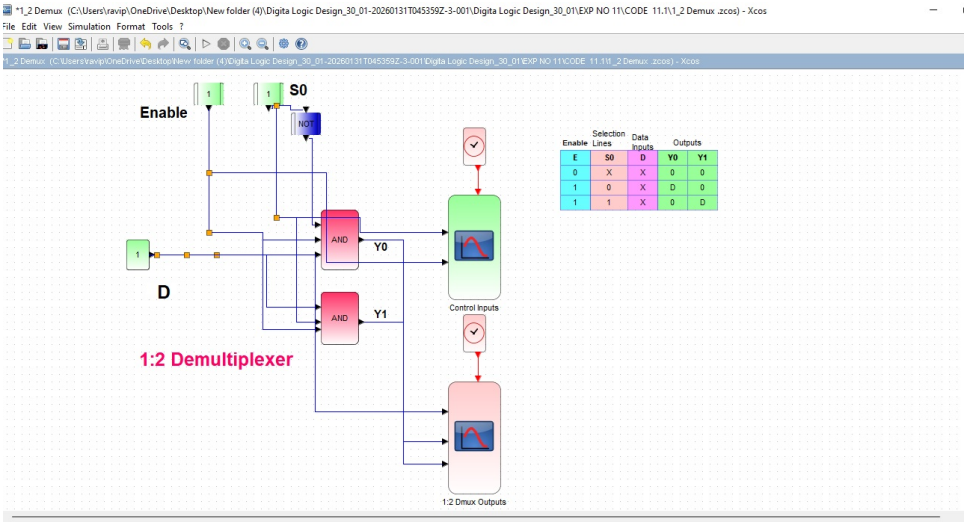

Figure 11.1: One as to Two DeMultiplexer

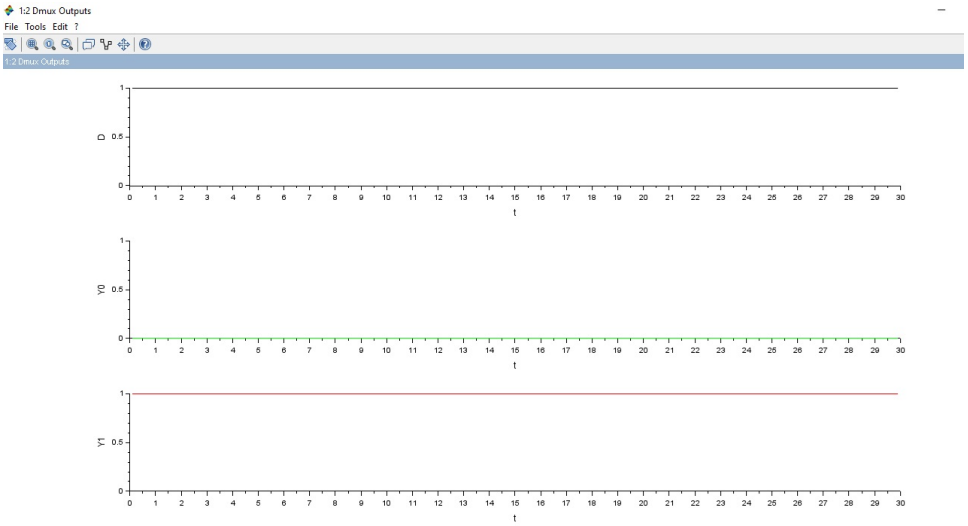

Figure 11.2: One as to Two DeMultiplexer

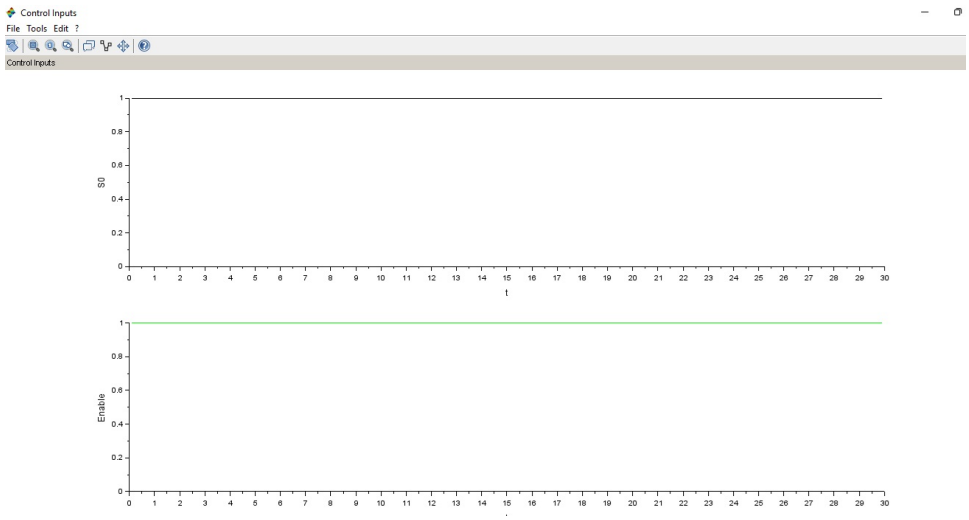

Figure 11.3: One as to Two DeMultiplexer

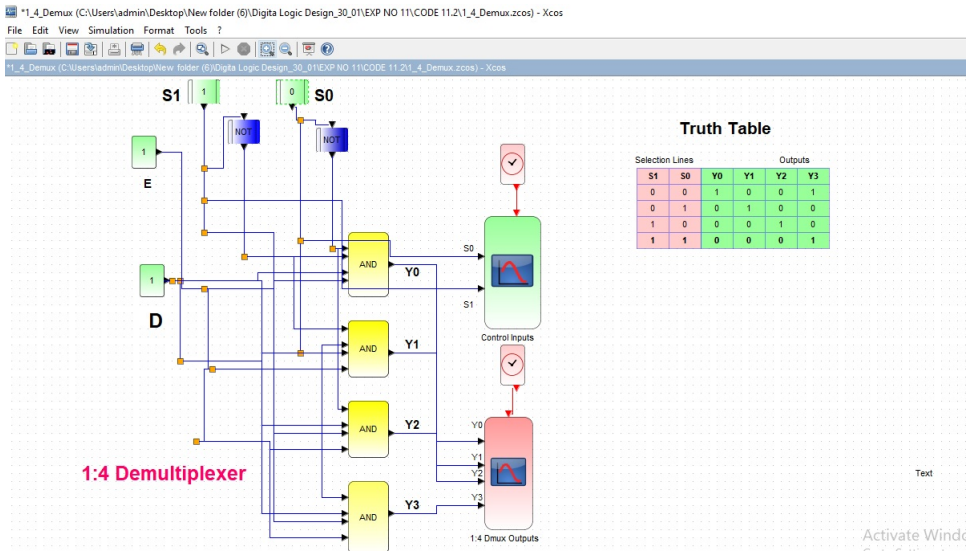

Figure 11.4: one as to Four Demux

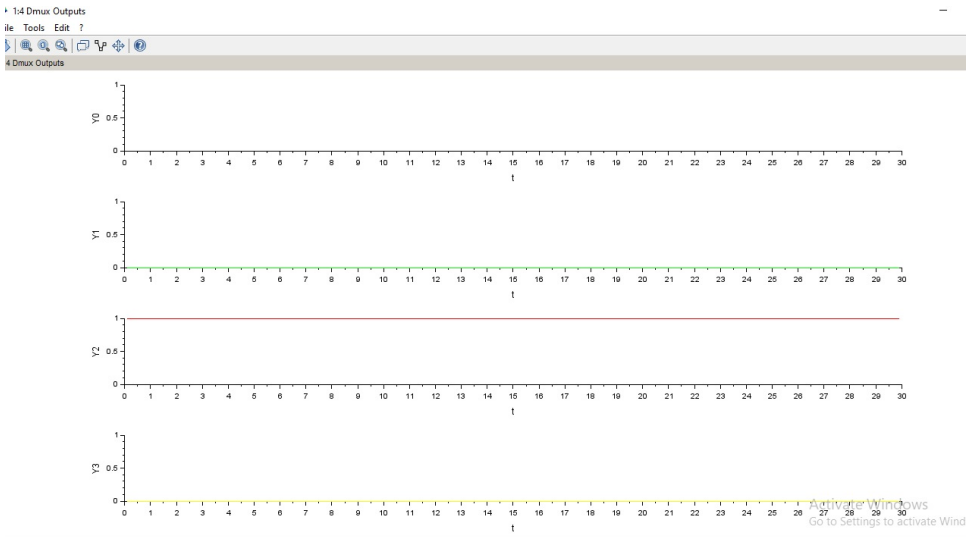

Figure 11.5: one as to Four Demux

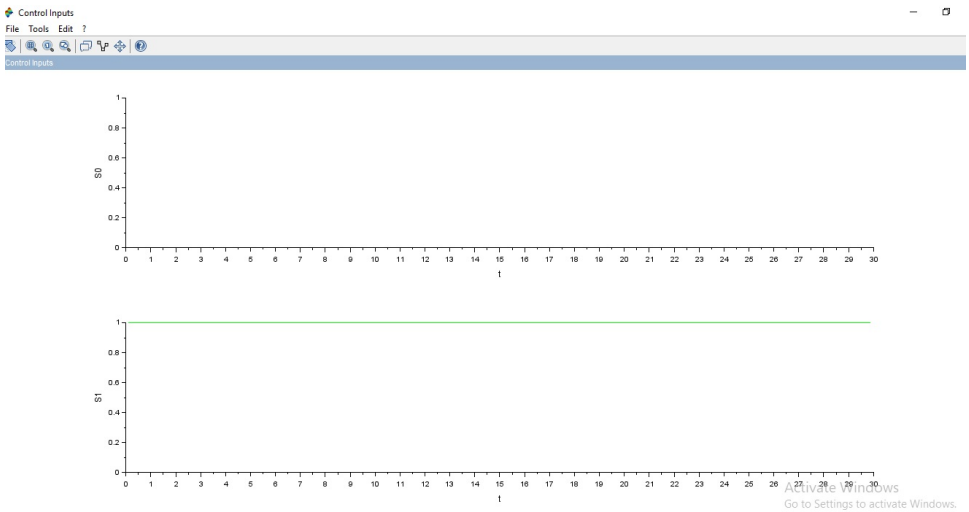

Figure 11.6: one as to Four Demux

Experiment: 12

Design and simulate SR and D types of flip flops.

This code can be downloaded from the website wwww.scilab.in

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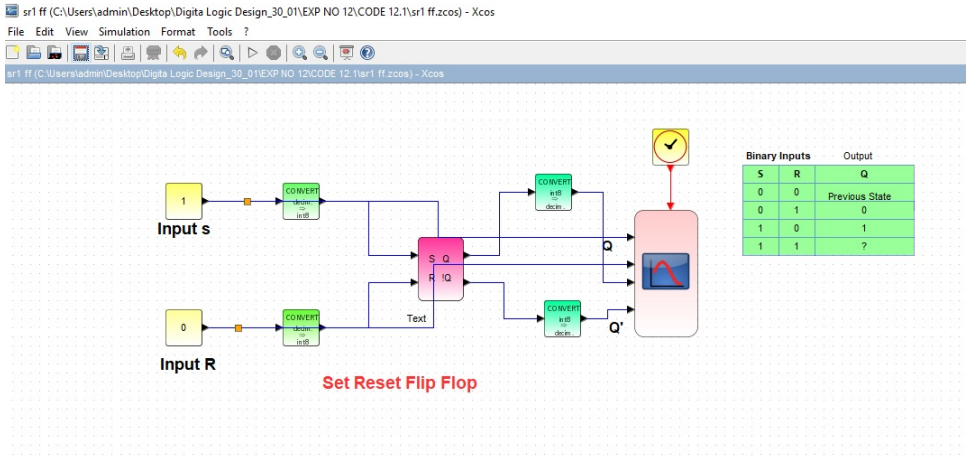

Figure 12.1: SR FF

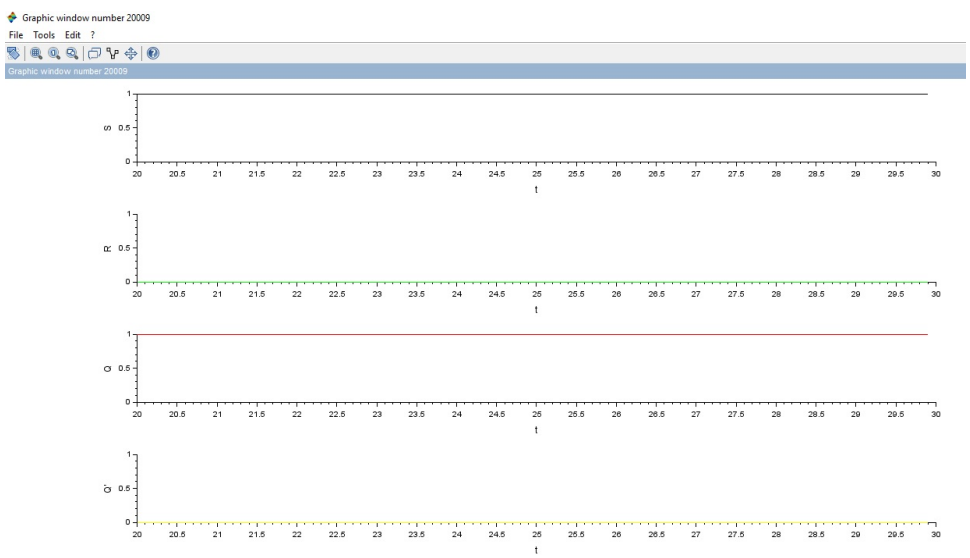

Figure 12.2: SR FF

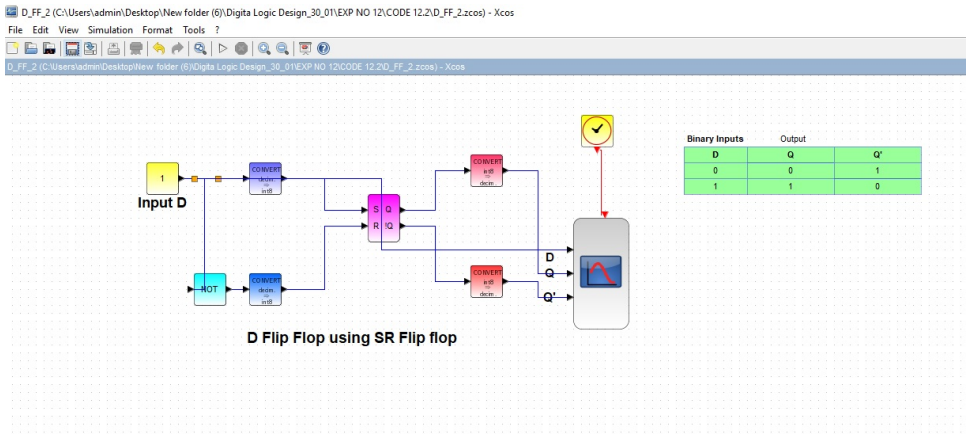

Figure 12.3: D FF

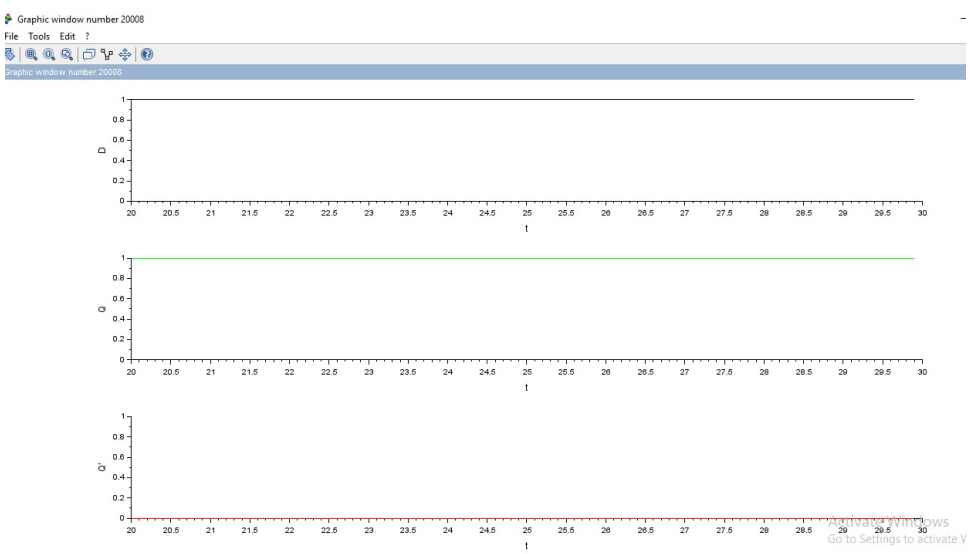

Figure 12.4: D FF